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(54) **IMAGE PROCESSING DEVICE AND METHOD THEREFOR, AND GAME MACHINE HAVING IMAGE PROCESSING PART.**

(57) In an access circuit (31) of a background picture generating part (22), cycle patterns are stored in an access register (40). Access commands read out are converted into control signals by a decoder (41). Addresses on a VRAM (12) which are assigned to necessary image data are generated by an address selector (42), and are fed to the VRAM (12). The image data are read from the VRAM (12) according to the control signals and the addresses, and they are stored in registers (33-36). Image data are read from the registers (33-36) by output circuits (37, 38), and picture element data are generated and outputted from the output circuits (37, 38). Thereby, alteration of the cycle patterns of the VRAM access can be treated flexibly which are resulted from alteration of display setting such as of the number of colors of the image data, the reduction ratios and the access frequencies. Further, according to the quantities of the image data and the access frequencies of the respective background pictures, the storages of the image data can be adjusted between a plurality of the VRAMs.

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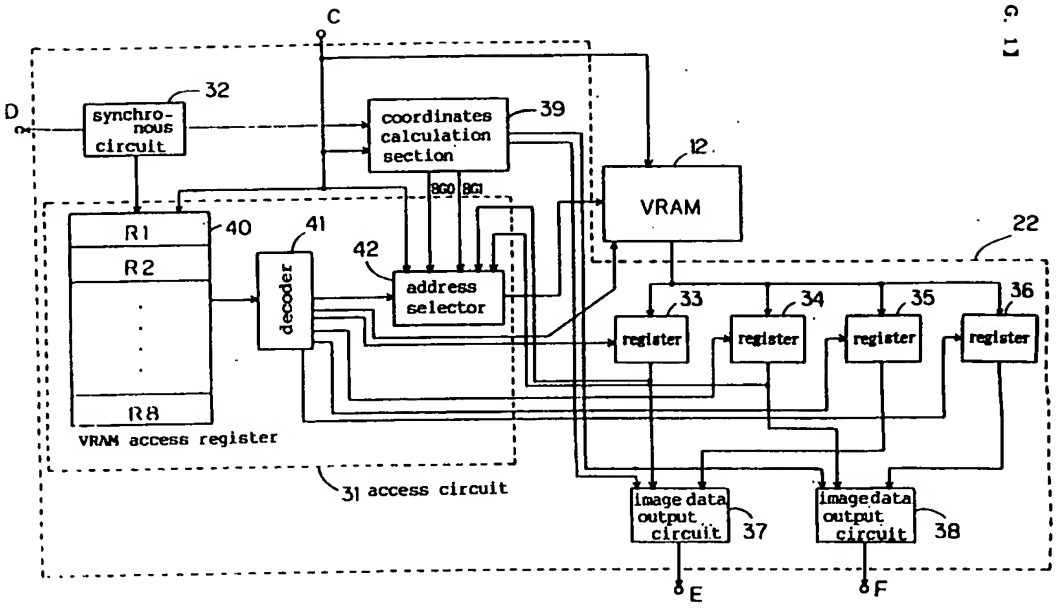
[FIG. 1]


C
D
synchro-nous circuit
32
coordinates calculation section
39
12
VRAM
22
R1
R2
R8
40
41
decoder
42
address selector
33
34
35
36
register
register
register
register
VRAM access register
31 access circuit
image data output circuit
37
image data output circuit
38
E
F

TECHNICAL FIELD

The present invention relates to an improved image processing circuit for generating background images in an image processing system.

BACKGROUND ART

Up to this time, an image displayed on a rasterscan monitor as in a video game consists of usually a plurality of background images (still pictures) forming a background, and a fore ground image (a dynamic picture) containing characters et cetera appearing in the video game and superimposed on the background images. These background images and foreground image have their respective priority levels (hereinafter referred to simply as priorities) for the output. Upon the superimposition, a highest priority image is only allowed to be displayed. The priorities are commonly indicated by predetermined numbers, with the images being displayed closer to the viewer in the ascending order of numbers. The numbers are typically assigned to each of the background images, as well as to each character of the foreground image.

Referring to Fig. 10(a), by way of example, are depicted a foreground image FG and two background images BG0 and BG1 each having numbers indicating priorities. In this case, "6" is assigned to a character CHR in the foreground image FG, and "2" and "4" to the background images BG0 and BG1, respectively. When superimposing, these images are viewed closer to the viewer in the order of the character CHR, back ground image BG1, and background image BG0, namely, in the order of descending priorities. In this manner, the background images forming a background picture and the foreground image forming a foreground picture are superimposed in synchronism in a predetermined sequence, thereby outputting an overall image as shown in Fig. 10(b) on a monitor screen.

[Conventional Example of Image Processing System]

In Fig. 11 is the prior image processing system for out putting the background images and foreground image described above. In Fig. 11, to a CPU 1 via a CPU interface 5 is connected a video processor 2 which is connected to a CRT display 16. To the CPU 1 is further connected to a storage unit 3 such as a CD-ROM or a ROM cartridge, and a RAM 4 providing a work area for the CPU 1.

The storage unit 3 stores programs for executing games and image data for displaying images for the video games. The image data are composed of the smallest unit called a pixel. And each pixel includes a color code as information, which specifies a color to be output by the predetermined number of bits, and a priority code which indicates an output priority. The storage unit 3 stores also voice data, data to specify specifying when and at which location the image data are to be displayed on the screen coordinates, and data specifying operations for rotation, movement, and scaling processing. The CPU 1 reads these data from the storage unit 3 to provide to the RAM 4, and transfers them by way of the CPU interface 5 to the video processor 2.

The video processor 2 includes a synchronous circuit 11 which generates synchronizing signals in synchronism with scanning of the CRT display 16. These synchronizing signals are generated and provided to components within the video processor 2 in order to output the foreground image and background images at the same timing. In addition to the synchronizing signals, image data for the foreground image and the background images are respectively transmitted to a foreground image processing section 6 and a background image processing section 7 under the control of the CPU 1.

To the foreground image processing section 6 are connected a command RAM 8 and a frame buffer 9. The command RAM 8 temporarily stores the transmitted image data for foreground image such as characters. Add the command RAM 8 stores, for example in a table format, commands given from the CPU 1 at the execution of a game program. The foreground image processing section 6 reads these commands from the command RAM 8, and for the execution stores them into an internal register. The foreground image processing section 6 reads the image data from the command RAM 8, performs on them various image processing such as coordinate calculations, scaling, and color operations, and writes the image data into predetermined addresses within the frame buffer 9. The image data expanded on the frame buffer 9 are output frame-by-frame to a priority circuit 12.

The image data for the background images forwarded to the background image processing section 7 are stored in a video RAM (hereinafter referred to as a VRAM) 10. The image data for the background images consist of pattern data and pattern Name data. As shown in Fig. 12(a2), the pattern data are each composed of an aggregate of color codes for respective pixels within a cell, the cell being a basic unit composed of for example 8 x 8 pixels in the horizontal and vertical directions as depicted in Fig. 12(a1). Also, the pattern name data contain data addresses of the above-described pattern data on the background images. As illustrated in Fig. 12(b), the background images are each comprised of an aggregate of a predetermined number of cells, and the pattern name data

specify the locations of cells on the background images being stored within the VRAM 10, by leading addresses of the cells on the VRAM.

Referring back to Fig. 11, the background image processing section 7, if needed, in accordance with a specification of the CPU 1, performs coordinate calculations and then image processing such as vertical or horizontal movement or rotations, and thereafter reads the image data from the VRAM 10 and transfers them to the priority circuit 12 by each background inage.

The priority circuit 12 checks the priorities in outputting foreground and background image data transferred respectively from the foreground image processing section 6 and the background image processing section 7, and outputs image data in the order of descending priorities to combine the foreground image and the background image, and forwards the results to a colorizing circuit 13.

A color RAM 14 is connected to the colorizing circuit 13. The color codes of the image data forwarded from the priority circuit 12 each specifies a specific address in conformity with which specific color data are read from the color RAM 14. These color data are converted into RGB data indicating a mixing ratio of three primary colors (red, green, blue) and delivered to a video signal generation circuit 15 in which the digital signals are converted into analog signals in the form of video signals by a D/A converter. The thus generated video signals are provided as output to the CRT display 16 such as a standard TV monitor.

[Access Circuit and VRAM Access In background image processing Section]

In the above video processor 2, the background image processing section 7 reads image data for background images from the VRAM 10. It also writes the image data for background images into the VRAM 10. These actions are called VRAM access, which are typically controlled by an access circuit 17 included in the background image processing section 7. The VRAM access will now be described.

To be concrete, the VRAM access is performed when reading the image data from the VRAM upon the display of background images and when writing new image data supplied from the CPU into the VRAM.

The VRAM access will include an "image data readout access" for reading out the image data stored in the VRAM, a "CPU access" for writing new image data from the CPU into the VRAM, and a "parameter readout access" for reading out parameters et cetera necessary for the image display stored in the VRAM.

The "image data readout access" is performed during the display period, in which predetermined access actions are specified to read out image data from the VRAM. These access actions consist of a "pattern name read" for specifying the readout of pattern name data within the VRAM, and a "pattern data read" for specifying the readout of pattern data.

The number of times of these access actions and the "CPU access" to be performed during the display period can be set as the contents of the VRAM access per unit time in accordance with predetermined restrictions.

As depicted in Fig. 13, the unit time for the VRAM access is typically a time taken to output one row (eight pixels) in the horizontal direction within a single cell, which is equivalent to one cycle. The access circuit serves to set one access for the output time of one pixel, thereby allowing the VRAM to be accessed eight times in one cycle. The contents of the eight VRAM access actions per one cycle are called a cycle pattern. During the display period, the access circuit selects addresses of the predetermined image data within the VRAM in accordance with the cycle pattern, and supplies these addresses to the VRAM, whereby the access to the VRAM can be controlled. For the CPU access to be set during the display period, there must be secured an access time for writing corresponding to the specified number of times. Referring to Fig. 14, concrete description will be given of an example of such VRAM access based on the cycle pattern in the case of using two background images BG0 and BG1.

[Conventional Example of VRAM Access]

Fig. 14(a) depicts, in a table format, a cycle pattern of the access circuit 17 included in the background image processing section 7 of Fig. 11. Fig. 14(b) depicts a data configuration contained in the VRAM 10 connected to the access circuit 17. In this case, cycle patterns for reading image data are previously set in the hardware. During the display period, the access circuit 17 reads pattern name data (PND) of the background image BG0 at the first access in accordance with a cycle pattern. Conventionally, in response to an instruction from the CPU, the access circuit 17 provides to the VRAM 10 a selection signal indicating an address of pattern name data of the background image BG0 within the VRAM. Then, in conformity with the address, the pattern name data for the background image BG0 are read from the VRAM 10.

Such access is commonly capable of reading image data for one complete word (16 bits) at a time. As shown in Fig. 14(c), the pattern name data are made up of 16 bits containing a leading ad-

dress of the pattern data (in units of cell) in the background image. Thus, by reading pattern name data of the BG0 at the first access, there can be obtained a leading address of corresponding pattern data of one cell on the background image BG0.

By the leading address of the pattern data thus obtained, the access circuit performs, at the second and subsequent access, readout of the pattern data (PTD) of the background image BG0 in accordance with the cycle pattern. In other words, the access circuit reads pattern data specified by the leading address and corresponding to one horizontal row (eight pixels) of a cell. Assuming that for both the background images BG0 and BG1, one word pattern data read by one access contains color codes for four pixels, the same pattern data must be accessed twice in order to read color codes for eight pixels. Therefore, read at the second and third access are pattern data of the background image BG0 corresponding to two words.

Also as to the background image BG1, pattern name data (PND) are read at fourth access to obtain a leading address of pattern data of the background image BG1. At the subsequent fifth and sixth access, the pattern data for two words (PTD) are read from the VRAM in conformity with the leading address. By repeating these contents of the first to sixth access, during the display period, image data of the background images BG0 and BG1 are successively read in the horizontal direction cell-by-cell in accordance with the cycle pattern.

In the case of the cycle pattern depicted in Fig. 14, the seventh and eighth access of one cycle (eight access actions) is composed of a CPU access for writing during the display period into the VRAM new image data supplied from the CPU. In this case, addresses of image data to be written are fed from the CPU into the VRAM 10. The image data written into the VRAM by the CPU access during the display period are read at appropriate timing in accordance with an image data readout procedure in the above-described cycle pattern. This will allow a background image to be rewritten in the process of a game to alter the background image.

As described above, the cycle patterns in the access circuit each serve to specify, as the contents of the access within a unit time, (1) timing to specify the access action during the display period and the number of times of the specification, and (2) the CPU access during the display period. A method has been hitherto employed in which these cycle patterns are previously set up in the hardware. More specifically, the hardware contains a plurality of cycle patterns as models fixed thereto in a predetermined data format, whereby a set of optimum data are selected from thereamong in accordance with a specification of the CPU.

[Variation In Amount of Image Data and Change of Cycle Pattern In VRAM Access]

Recent video games have a tendency to emphasize a visual effect in playing the games in addition to natures of story the games possess. With this tendency, in order to arouse players' interest in the game, a measure is indispensable for providing a more beautiful image using multiple colors while complicating both dynamic change in movement or rotation and change in scaling. The above device includes more detailed setting of conditions for display, for example, by increasing the number of background images to be used or by individually varying the number of colors or the scaling factor to be used for each of the background images. On the contrary, however, such complicated setting of conditions may result in a remarkable increase in the amount of information contained in the image data of the background image.

As depicted in Fig. 15(a), by way of example, a background image BG0 makes use of 16 colors for displaying only color letters or numbers such as scores, while a background image BG1 employs 256 colors for displaying a floridly colored background image. In this case, to specify color data within the color RAM, color codes per pixel in the pattern data each require the amount of data of four (4) bits and eight (8) bits, respectively, for the 16 colored background image BG0 and for the 256 colored background image BG1. In this manner, increase in the number of colors for use will lead to the increased amount of data per pixel, and therefore the increased amount of information (number of bits) in the pattern data.

Such variation in the amount of information of the image data will affect the setting of cycle patterns in the VRAM access. Referring to Fig. 15-(b), the color code per pixel is four (4) bits and eight (8) bits, respectively, in the background images BG0 and BG1. When reading one word pattern data by one access in a cycle pattern, the one word (16 bits) contains color codes for four pixels with respect to the background image BG0, whereas it merely includes color codes for two pixels with respect to the background image BG1. Thus, in order to read the predetermined amount of pattern data (which correspond to eight pixels in a horizontal row of a cell), the background image BG0 simply requires that two access times be set in a cycle pattern, whereas the background image BG1 needs the setting of four access times, namely more access times per cycle pattern. In this manner, occurrence of variance in the amount of

information of image data will cause a necessity to accordingly change the setting of the cycle pattern.

[Increase in Amount of Image Data and Setting of VRAM Capacity]

Against the increased amount of information of image data in this manner, the following measures have been hitherto taken in addition to changing the cycle pattern. As a measure for reading out maximal image data from the VRAM by a single access in the VRAM access, a method was often employed in which a plurality of separate VRAM's are connected to the background image processing section, all the VRAM's being simultaneously accessed with individual VRAM's assigned to respective background images. Alternatively, a method was also employed in which a single VRAM is divided into a plurality of portions called banks, all the banks being accessed at the same time, with each bank assigned to each background image.

However, the above-described prior art involved the following problems. As stated above, if the conditions on display such as the number of colors used are set in detail to improve the image representation of the background images, the cycle pattern upon the VRAM access also undergoes changes such as increase or decrease in the number of times of access. In such case, the conventional access method generally employed a method in which an optimum combination is selected from among a plurality of setting conditions which has been previously assumed. For instance, a method was employed in which predetermined data formats each representing a cycle pattern to be a model are individually numbered for the storage in a register so that the CPU can specify the number. However, this entailed a deficiency that the number of possible combinations is troublesomely increased accordingly as the number of scroll screens and the kind of setting such as the number of colors or size reduction are increased. It was also possible to employ a method in which an optimum pattern is determined by the hardware instead or being selected from the combinations, which may disadvantageously result in an increased circuit scale and an excessive load onto the hardware.

In order to deal with the problem of increased amount of information of the image data to be written from the CPU, which will lead to a deficiency in write time, the CPU must be accessed as frequently as possible by effectively utilizing free time in the hardware access during the display period. It was however difficult in the conventional access circuit to flexibly set the CPU access time as needed since the access pattern which has been once determined were fixed unchangingly. In this manner, the conventional method in which the access patterns are fixedly set in the hardware had numerous restrictions to display a plurality of background images each having individual display setting.

The VRAM intended to store and read the image data, on the other hand, presented the following inconveniences arising from its fixed capacity to be used. In the case where a plurality of VRAM's having the same capacity were provided, all the VRAM's were difficult to effectively use. This example is shown using Fig. 16. A couple of VRAM's, VRAM-A and VRAM-B are respectively assigned to background images BG0 and BG1. Assume herein that the background image BG1 is not displayed at all in scene A of a game, but appears in scene B of the same game. In this case, the capacity of the VRAM-B for the background image BG1 in the scene A is merely a "necessary waste" actually out of use although it has been preset allowing for the possible use. Also, regardless of a plenty of image data in the background image BG0, the VRAM-B is not permitted to be used for the background image BG0. The same applies to the case where a single VRAM is divided into a plurality of banks. In this manner, the conventional use of the VRAM capacity did not find a method providing an effective regulation for the VRAM capacity in accordance with the amount of image data which the respective background images contain as well as the conditions under which the background images are used.

The present invention was conceived in view of the above problems, a first object of which is to provide an image processing method capable of flexibly changing access actions within a unit time in a VRAM access in accordance with changes in display setting such as the number of colors of image data, a size reduction ratio, or an access frequency, without increasing an burden on the hardware.

A second object of the present invention is to provide an image processing method capable of, in accordance with the amount of image data of each background image and the access frequency, controlling the storage of the image data among a plurality of VRAM's.

A third object of the present invention is to provide an image processing method allowing the realization of the third object not merely between the plurality of VRAM's but also between a plurality of banks of the same VRAM.

A fourth object of the present invention is to provide an image processing system capable of setting and changing the access actions within a unit time in the VRAM access under the control of a CPU, and of distinctively outputting background images having different display conditions.

A fifth object of the present invention is to provide an image processing system ensuring an automatic and smooth execution in sequence of access actions within a preset unit time in the VRAM access.

A sixth object of the present invention is to provide an image processing system in which addresses of the image data on the VRAM are generated by calculation and selected for the supply to the VRAM in the VRAM access.

A seventh object of the present invention is to provide an image processing system having a configuration capable of specifying a predetermined action in the VRAM access and of executing the action promptly.

Ad eighth object of the present invention is to provide an image processing system realizing the seventh object without burdening the memory capacity.

A ninth object of the present invention is to provide an image processing system having a concrete configuration allowing an easy setting and change of VRAM access actions within a predetermined unit time.

A tenth object of the present invention is to provide an image processing system having a concrete configuration capable of controlling the VRAM access actions within the predetermined unit time by means of the CPU.

Ad eleventh object of the present invention is to provide an image processing system having a concrete configuration ensuring an automatic and smooth execution in sequence of access actions to the VRAM.

A twelfth object of the present invention is to provide an image processing system capable of easily implementing, under the control of the CPU, a configuration for allocating the VRAM capacity to the image data as well as changing the allocation.

A thirteenth object of the present invention is to provide an image processing system capable of setting and changing, under the control of the CPU, the access actions within a unit time in the VRAM access and capable of distinctively outputting the background images having different display conditions.

A fourteenth object of the present invention is to provide a game machine ensuring an automatic and smooth execution in sequence of access actions within a preset unit time in the VRAM access.

A fifteenth object of the present invention is to provide a game machine of a type in which addresses of image data on the VRAM are generated by calculation and selected for the supply to the VRAM in the VRAM access.

A sixteenth object of the present invention is to provide a game machine having a configuration capable of specifying a predetermined action in the VRAM access as well as of executing the action promptly.

A seventeenth object of the present invention is to provide a game machine accomplishing the sixteenth object without burdening the memory capacity.

An eighteenth object of the present invention is to provide a game machine having a concrete configuration capable of easily setting and changing the VRAM access actions within a predetermined unit time.

An nineteenth object of the present invention is to provide a game machine having a concrete configuration capable of controlling the VRAM access actions within a predetermined unit time by the CPU.

A twentieth object of the present invention is to provide a game machine having a concrete configuration in which the access to the VRAM is automatically and smoothly executed in sequence.

A twenty-first object of the present invention is to provide a game machine implementing, under the control of the CPU, a configuration for allocating the VRAM capacity to the image data and setting the change of the allocation.

SUMMARY OF THE INVENTION

As a means for solving the above problems, according to a first aspect of the present invention defined in claim 1, there is provided an image processing method in which image data for forming a foreground image are stored into a frame buffer while simultaneously storing image data for forming background images into a video RAM and in which the image data for a foreground image are read from the frame buffer in a foreground image processing section in synchronism with the read of the image data for background images from the video RAM in a background image processing section, whereby at the same timing the foreground image and background images are generated and superimposed with each other to be output in the form of a synthetic image, the method comprising the steps of specifying the contents of concrete actions to be imparted to the video RAM in order to perform read and write of the background image data, setting the specified contents of actions at given unit time intervals, the setting being instructed by a CPU, and accessing the video RAM in conformity with an instruction from the CPU.

The invention defined in claim 2 provides an image processing method in which one ore more video RAM's are provided for storing image data for background images and in which the video RAM's store image data and are simultaneously accessed, the method comprising the steps of by means of a CPU, specifying the read of the video

RAM's and image data stored in the video RAM's.

In the invention defined in claim 3, the video RAM defined in claim 2 is segmented into two banks which are plurality of RAM portions each having the same capacity, and the CPU specifies the read of the banks and image data stored in the banks.

According to a second aspect of the present invention defined in claim 4, there is provided an image processing system including a foreground image processing means which stores image data for forming a foreground image into a RAM and develops the image data into a frame buffer and at a predetermined timing reads out the image data for a foreground image from the frame buffer, a background image processing means which reads out image data for forming background images from a video RAM, a priority determining means which determines display priority among image data for a foreground image transferred from the foreground image processing means and image data for background images transferred from the background image processing means, and an output means which outputs the image data for a foreground image and background images in conformity with the priority, the system comprising, a specifying means for specifying actions reading or writing image data stored in the video RAM; a first setting means for setting at given unit time intervals the actions specified by the specifying means, a storage means for storing the contents of the actions set at given unit time intervals by the first setting means, an access control means for controlling access to the video RAM in compliance with the contents stored it the storage means, and a bit-number output control means for performing output control by the number of bits of predetermined data within image data in accordance with the amount of information differing for each of background images.

In the invention defined in claim 5, the access con trol means defined in claim 4 includes a conversion means for converting a specification by the specifying means into a control signal, and an address selection means for selecting an address on the video RAM of image data read out from the video RAM.

In the invention defined in claim 6, the address selection means defined in claim 5 includes a first generation means for generating an address on the video RAM of pattern name data, and a second generation means for generating an address on the video RAM of pattern data.

According to the invention defined in claim 7, in a video RAM access for reading image data for background images by accessing the video RAM storing as the image data both pattern data composed of predetermined number of pixel informations and pattern name data for designating positions in the background images of the pattern data defining images to be displayed, the image processing system defined in claim 4 uses an access command as a specification means for specifying the action reading or writing the pattern data or pattern name data.

In the invention defined in claim 8, the access command defined in claim 7 is a binary code consisting of a predetermined number of bits.

According to the invention defined in claim 9, in the video RAM access, the image processing system defined in claim 7 sets a cycle pattern in the form allowing read-in by the CPU as a setting means for setting in one cycle unit during the display period the action specified by the access command.

According to the invention defined in claim 10, in the video RAM access, the image processing system defined in claim 7 uses a video RAM access register as a storage means for storing the cycle pattern.

According to the invention defined in claim 11, in the video RAM access, the image processing system defined in claim 7 executes access to the video RAM in conformity with the access command sequentially read from the cycle pattern stored in the access register.

According to the invention defined in claim 12, in the case of using a plurality of video RAM's or a plurality of banks for storing image data for background images, the image processing system defined in claim 4 further comprises a second setting means for setting whether the video RAM is to be divided into a plurality of banks or not, and an access means allowing simultaneous access to the plurality of video RAM's or to the plurality of banks, by allocating a plurality of the storage means to each of the plurality of video RAM's or each of the plurality of banks of the video RAM.

According to a third aspect of the present invention defined in claim 13, there is provided a game machine including a foreground image processing means which stores image data for forming a foreground image into a RAM and develops the image data into a frame buffer and at a predetermined timing reads out the image data for a foreground image from the frame buffer, a background image processing means which reads out image data for forming background images from a video RAM, a priority determining means which determines display priority among image data for a foreground image transferred from the foreground image processing means and image data for background images transferred from the background image processing means, and an output means which outputs the image data for a foreground image and background images in conformity with

the priority, the game machine comprising a specifying means for specifying actions reading or writing image data stored in the video RAM, a first setting means for setting at given unit time intervals the actions specified by the specifying means, a storage means for storing the contents of the actions set at given unit time intervals by the first setting means an access control means for controlling access to the video RAM in compliance with the contents stored in the storage means, and a bit-number output control means for performing output control by the number of bits of predetermined data within image data in accordance with the amount of information differing for each of background images.

In the invention defined in claim 14, the access control means defined in claim 13 includes a conversion means for converting a specification by the specifying means into a control signal, and an address selection means for selecting an address on the video RAM of image data read out from the video RAM.

In the invention defined in claim 15, the address selection means defined in claim 14 includes a first generation means for generating an address on the video RAM of pattern name data, and a second generation means for generating an address on the video RAM of pattern data.

According to the invention defined in claim 16, in a video RAM access for reading image data for background images by accessing the video RAM storing as the image data both pattern data composed of predetermined number of pixel informations and pattern name data for designating positions in the background images of the pattern data defining images to be displayed, the game machine defined in claim 13 uses an access command as a specification means for specifying the action reading or writing the pattern data or pattern name data.

In the invention defined in claim 17, the access command defined in claim 16 is a binary code consisting of a predetermined number of bits.

According to the invention defined in claim 18, in the video RAM access, the game machine defined in claim 16 sets a cycle pattern in the form allowing read-in by the CPU as a setting means for setting in one cycle unit during the display period the action specified by the access command.

According to the invention defined in claim 19, in the video RAM access, the game machine defined in claim 16 uses a video RAM access register as a storage means for storing the cycle pattern.

According to the invention defined in claim 20, in the video RAM access, the game machine accesses the video RAM in conformity with the access command sequentially read from the cycle pattern stored in the access register.

According to the invention defined in claim 21, in the case of using a plurality of video RAM's or a plurality of banks for storing image data for background images, the game machine defined in claim 13 further comprises a second setting means for setting whether the video RAM is to be divided into a plurality of banks or not, and an access means allowing simultaneous access to the plurality of video RAM's or to the plurality of banks, by allocating a plurality of the storage means to each of the plurality of video RAM's or each of the plurality of banks of the video RAM.

Description will now be given of operations of the present invention having the above configuration.

In order to set a cycle pattern of VRAM access, it is necessary to set conditions on the image data display for each of the background images. More specifically, the conditions include the number of colors used in each background image, scaling, the presence or absence of CPU access, and on-VRAM storage locations of image data required for each background image.

Based on these conditions, a cycle pattern of access to the VRAM for reading and writing image data is set for each of VRAM's arranged. That is, decided are access commands needed for one cycle, the number of times of access actions by these commands, and access timing.

According to the invention defined in claim 1, a cycle pattern set in conformity with the above conditions is prepared in a software or a ROM, the contents being read by a CPU upon the execution of a game so as to allow a specification or change.

According to the invention defined in claim 2, predetermined image data to be stored in each VRAM are set in advance, and the read of the image data can be specified by using the cycle pattern which is read by the CPU upon the execution of the game.

The above processing can be more freely set by a programmer familiar with the contents of a game program or various data and conditions used in the program. It is thus possible to set proper conditions, resulting in increased efficiency. Also, when changing such setting, it is merely required to change the software or ROM. This will allow an easy change of use of an idle area in the access time or VRAM capacity. Therefore, useless access time or useless VRAM capacity can be saved which have been hitherto fixedly set in the hardware regardless of possible no use.

In this manner, the inventions defined in claims 1 and 2 ensure a flexible dealing with the amount of information of the image data which may vary with time by scenes in the process of a game or

with the change in the state of use of the VRAM.

The invention defined in claim 3 ensures an effective utilization of the limited VRAM capacity as well as read of plenty of image data from the VRAM. First, it is effective since either bank division or use of a single VRAM can be selected in accordance with the amount of information of the image data. Second, plenty of image data can be read since a single VRAM is divided into a plurality of banks having the same capacity which are simultaneously accessed. Also, allocation of image data of each background image to each bank would contribute to the increased number of background images to be displayed at one time. Third, use of the cycle pattern setting would allow a rational allocation of the VRAM capacity since it is possible to freely increase or decrease banks to be allocated to image data or the number of the banks.

The invention defined in claim 4 realizes an image processing system capable of flexibly changing, as needed, a cycle pattern in the VRAM access. The specifying means specifies an access action it the VRAM. Then, using the specifying means, the first setting means sets the contents of the access actions to be performed it a given unit time, and keeps the thus set contents of access in the form capable of being read into the CPU. The CPU stores the read-in contents of access into the storage means. Further, the access control means controls the VRAM access referring to the stored contents of access. At that time, the output bit control means performs an allocating operation based on the number of bits of image data in order to ensure a correct output of a plurality of background images whose respective image data have different amount of information. Thus, image data of the same background image can be output together.

In the image processing system, according to the invention defined in claim 5, there can be obtained a configuration in which the contents of the access actions are read from the storage means in the VRAM access so that the access is controlled in accordance with the contents. More specifically, the information of the contents of access written into the storage means are divided into two portions, one for the kind of image data specified, the other for the specification of read and write, which are in synchronism transferred through two different paths to the VRAM. That is, the conversion means generates a read/write signal from the information of the access command, and designates the read or write of the specified image data. Then the address selection means selects an address on VRAM of the specified image data, and delivers it to the VRAM. The VRAM receives the address of the image data and the read/write signal to read the specified image data, and thereafter stores the image data into a predetermined data buffer.

In the processing system, according to the invention defined in claim 6, by the kind of image data there can be generated addresses on VRAM of image data required for the read of the image data from the VRAM or for the write into the VRAM. More specifically, if the access command is "pattern name read", the first generation means generates the addresses on VRAM of the pattern name data and supplied them to the VRAM. On the contrary, if the access command is "pattern data read", the second generation means generates addresses on VRAM of the pattern data and supplies them to the VRAM.

In the VRAM access of the image processing system, according to the invention defined in claim 7, a predetermined access command is used as a specification means representing access actions such as read or write of both the pattern data which are image data of the background image to be stored in the VRAM and the pattern name data. This will allow a simple representation of each access action, contributing to a simple specification of setting or change in the access actions.

According to the invention defined in claim 8, use is made of a code having a predetermined number of bits as an access command in the image processing system. This saves the memory capacity within the image processing system. Further, the command is read in the form of a binary code, ensuring a prompter execution of the access actions.

In the VRAM access of the image processing system, according to the invention defined in claim 9, cycle patterns can be effectively and collectively set in the form allowing a read-in by the CPU, for example, in a CD-ROM, the cycle patterns each being a series of access actions set for each cycle during the display period.

According to the invention defined in claim 10, the cycle patterns in the image processing system are stored in the VRAM access registers, allowing the control of the read and write by the CPU.

In the image processing system, according to the invention defined in claim 11, there can be obtained an automatic mechanism in which the access circuit reads access commands in sequence from the cycle pattern for smooth execution.

The invention defined in claim 12 realizes a concrete image processing system allowing an effective use of the VRAM capacity. That is, the second setting means sets whether the VRAM is to be divided into a plurality of banks or not. As a result of this, it can be determined depending on the amount of image data whether the whole of the

VRAM capacity is to be used or a part thereof is to be used. Further, the access means accesses the VRAM or the VRAM banks at the same time. To be concrete, for each of VRAM's or the VRAM banks provided, a cycle pattern is set in accordance with the display conditions such as the amount of information of the image data stored therein and access frequency. This will accomplish a simultaneous display of a plurality of background images, and an increase in the amount of image data to be read, and an effective use of VRAM capacity.

The invention defined in claim 12 implements a game machine capable of flexibly changing, as needed, a cycle pattern in the VRAM access. That is, the specifying means specifies the access action in the VRAM. Then, using the specifying means, the first setting means sets the contents of the access actions to be performed in a given unit time, and keeps the thus set contents of access in the form capable of being read into the CPU. The CPU stores the read-in contents of access into the storage means. Further, the access control means controls the VRAM access referring to the stored contents of access. At that time, the output bit control means performs an allocating operation based or the number of bits of image data in order to ensure a correct output of a plurality of background images whose respective image data have different amount of information. Thus, image data of the same background image can be output together.

In the game machine, according to the invention defined in claim 14, there can be obtained a configuration in which the contents of the actess actions are read from the storage means in the VRAM access so that the access is controlled in accordance with the contents. More specifically, the information of the contents of access written into the storage means are divided into two portions, one for the kind of image data specified, the other for the specification of read and write, which are in synchronism transferred through two different paths to the VRAM. That is, the conversion means generates a read/write signal from the information of the access command, and designates the read or write of the specified image data. Then the address selection means selects an address on VRAM of the specified image data, and delivers it to the VRAM. The VRAM receives the address of the image data and the read/write signal to read the specified image data, and thereafter stores the image data into a predetermined data buffer.

In the game machine, according to the invention defined in claim 15, by the kind of image data there can be generated addresses on VRAM of image data required for the read of the image data from the VRAM or for the write into the VRAM. More specifically, if the access command is "pattern name read", the first generation means generates the addresses on VRAM of the pattern name data and supplied them to the VRAM. On the contrary, if the access command is "pattern data read", the second generation means generates addresses on VRAM of the pattern data and supplies them to the VRAM.

In the VRAM access of the game machine, according to the invention defined in claim 16, a predetermined access command is used as a specification means representing access actions such as writeout or read-in of both the pattern data which are image data of the background image to be stored in the VRAM and the pattern name data. This will allow a simple representation of each access action, contributing to a simple specification of setting or change in the access actions.

According to the invention defined in claim 17, use is made of a code having a predetermined number of bits as an access command in the image processing system. This saves the memory capacity within the image processing system. Further, the command is read in the form of a binary code, ensuring a prompter execution of the access actions.

In the VRAM access of the game machine, according to the invention defined in claim 18, cycle patterns can be effectively and collectively set in the form allowing a read-in by the CPU, for example, in a CD-ROM, the cycle patterns each being a series of access actions set for each cycle during the display period.

According to the invention defined in claim 19, the cycle patterns in the image processing system are stored in the VRAM access registers, allowing the control of the read and write by the CPU.

In the game machine, according to the invention defined in claim 20, there can be obtained an automatic mechanism in which the access circuit reads access commands in sequence from the cycle pattern for smooth execution.

The invention defined in claim 12 realizes a concrete game machine allowing an effective use of the VRAM capacity. That is, the second setting means sets whether the VRAM is to be divided into a plurality of banks or not. As a result of this, it can be determined depending on the amount of image data whether the whole of the VRAM capacity is to be used or a part thereof is to be used. Further, the access means accesses the VRAM or the VRAM banks at the same time. To be concrete, for each of VRAM's or the VRAM banks provided, a cycle pattern is set in accordance with the display conditions such as the amount of information of the image data stored therein and access frequency. This will accomplish a simultaneous display of a plurality of background images, and an increase in the amount of image data to be read, and an

effective use of VRAM capacity.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a clock diagram depicting a configuration of a background image generation section in an embodiment of the present invention;
Fig. 2 is a block diagram depicting a configuration of an image processing system in the embodiment of the present invention;
Fig. 3 is a block diagram depicting a configuration of a scroll engine in the embodiment of the present invention;
Fig. 4 depicts a cycle pattern to be set in the embodiment;
Fig. 5 depicts procedures for generating a pattern name address in the embodiment of the present invention;
Fig. 6 depicts procedures for generating a pattern data address in the embodiment of the present invention;
Fig. 7 illustrates procedures for generating pixel data in an output circuit of the present invention;
Fig. 8 illustrates additional provision and setting of an access register and a VRAM in reference example 1 of the present invention;
Fig. 9 illustrates changes in allocation of a VRAM capacity in reference example 2 of the present invention;
Fig. 10 illustrates procedures for outputting a foreground image and background images in the image processing system;
Fig. 11 is a conceptual diagram of a conventional image processing system;
Figs. 12(a1) and 12(a2) are diagrams showing a configuration of a cell and pattern data;
Fig. 12(b) is a diagram showing locations of cells on a background image;
Fig. 13 is a diagram showing a unit time (cycle) upon VRAM access;
Fig. 14 is an explanatory diagram for the VRAM access;
Fig. 15 is a diagram showing a relationship between the number of colors used and the number of bits of a color code per pixel; and
Fig. 16 is a diagram showing procedures for changing an allocation of the VRAM capacity to the image data.

BEST MODE FOR CARRYING OUT THE INVENTION

An embodiment of an image processing system according to the present invention will now be described with reference to the accompanying drawings. Description of the present embodiment follows the table of contents below.

⟨Present Embodiment⟩ Table of Contents

1. Overall Configuration of Present Embodiment

Referring first to Fig. 2, description will be given of a configuration of an image processing system including a background image processing section of the present invention. Assumed in the present embodiment are display screens for a foreground image and for a background image, on which images formed from image data are displayed. Among these display screens, one for the foreground image is referred to as a sprite screen, and one for the background images is referred to as a scroll screen.

1-1 Overall Configuration of Image Processing System of present Embodiment

Fig. 2 is a block diagram depicting an embodiment of an image processing system according to the present invention. In Fig. 2, a CPU 1, a RAM 2, and a video processor 3 are linked to a bus 14 whose use permission is controlled by a bus controller 13. The video processor 3 comprises a sprite engine 5, scroll engine 6, and a D/A converter 7. To the sprite engine 5 are coupled a command RAM 8 and a frame buffer 9. A scroll engine 6 includes therewithin a color RAM 10 and a variety of registers 11, and is coupled to a VRAM 12. Functions of the scroll engine 6 are set in the registers 11 by the CPU 1. Associated with this embodiment are, for example, a VRAM access register intended to store cycle patterns for controlling VRAM access actions during a display period, and a register for specifying whether or not the VRAM is to be divided into a plurality of banks. A monitor 4 is coupled to the video processor 3.

The CPU 1 stores into the RAM 2 a game program read from an external storage unit (not shown) such as a CD-ROM, and transfers to the video processor 3 read output image data together with commands or instructions needed for image processing. In the video processor 3, the sprite engine 5 serving as an image processing section for foreground temporarily stores in the form of a command table in the command RAM 8 a foreground command transferred from the CPU 1. The command is read by the sprite engine and set in an internal system register for execution. In the command RAM 8 are further stored image data for foreground also transferred from the CPU 1. The sprite engine 5 reads the image data from the command RAM 8 for image processing such as rotation, scaling and color operation. Afterwards, the image data are written into predetermined addresses on the frame buffer 9 to develop a dynamic picture for a foreground image. The image data for background image FG in the frame buffer 9 are read in sequence by the sprite engine 5, and supplied to the scroll engine 6 directly without using the bus 14.

Fig. 3 depicts a configuration of the scroll engine 6 for forming background images. As shown in Fig. 3, the image data of the sprite engine 5 in Fig. 2 are fed to the scroll engine by way of an terminal A. The scroll engine 6 comprises a window control section 21 for window processing on the sprite and scroll screens, a background image generation section 22 (described later) for processing the image data on the scroll screen, and a display control section 23. The display control section 23 includes a priority circuit 24 and a colorization circuit 25. With respect to the image data for foreground image and background image read in the background image generation section 22, the display control section 23 judges an output priority on pixel-by-pixel basis to synthesize an image. The image data are further colorized by a color RAM 10 coupled thereto. The thus processed image data are transferred, along with RGB data generated in the colorization circuit 25, through a terminal B to the D/A converter 7 of Fig. 2. In the D/A converter 7 the image data are converted into color video signals in analog representation, and then fed to the display 4 represented by a standard TV monitor.

1-2 Configuration In Background Processing Section of Present Embodiment

In Fig. 3 depicting the configuration of the scroll engine 6 within the video processor 3, the background image generation section 22 in particular is characterized in that it includes therewithin a variety of registers 11 allowing writing from the CPU 1 so as to perform both the control of VRAM access and the regulation of VRAM capacity to be allocated to the image data. For the control of the VRAM access in the display period, a VRAM access register is provided to allow the CPU to write the contents of access actions within one cycle (a cycle pattern) to be executed during the display period of the image data. Referring to Fig. 1, with a particular notice on the function at the time of VRAM access, description will be given of a configuration of the background image generation section 22 which is a circuit according to the present invention.

In Fig. 1, the background image generation section 22 is coupled to the VRAM 12 and comprises an access circuit 31 for controlling the VRAM access, a synchronous circuit 32, data buffers (registers 33 to 36) for temporarily storing image data to be read from the VRAM until they are output, image data output circuits (37 and 38), and a coordinate calculation section 39 for controlling the movement such as vertical and horizontal movement and rotation of the scroll screen.

The access circuit 31 includes a VRAM access register 40, a decoder 41, and an address selector 42. A terminal C is linked to the CPU 1 to allow the supply of commands from a game program, image data, addresses of the image data and so on.

The synchronous circuit 32 generates horizontal and vertical synchronizing signals in synchronism with the scan of the monitor 4 as well as synchronizing signals on dot-by-dot basis. These synchronizing signals are fed through a terminal D to the sprite engine while simultaneously being supplied via the coordinate calculation section 39 to each parts of the back ground image generation circuit 22. This will allow the coincidence of position and timing in the output of the foreground images and background image. The synchronous circuit 32 further generates address signals of one dot (pixel) cycle and supplies them to the VRAM access registers. The image data on pixel-by-pixel basis generated in the image data output circuits 37 and 38 within the background image generation circuit 22 are provided as output to the display control section 23 of Fig. 3 by way of terminals E and F.

2. Operation and Effect of Present Embodiment

The following is a description on the operation of the background image processing section according to the present embodiment having the above configuration.

2-1 Setting of Display Conditions

In the access circuit 31 of Fig. 1, the following conditions by way of example need to be preset prior to the setting of a cycle pattern designating the contents of VRAM access within a unit time (one cycle).

(1) Display conditions such as the number of scroll screens for display, the number of colors used by each scroll screen, and setting of size reduction.

(2) Allocation of the capacity of the VRAM storing image data for each scroll screen, - the number of VRAM's used, and the bank is to be divided or not -

(3) CPU access is to ba performed or not.

This embodiment employs two scroll screens BG0 and BG1 for display, the scroll screen BG0 using 16 colors and the scroll screen BG1 using 256 colors. Also assume that these scroll screens are subjected to no size reduction, and that a single VRAM is not divided for use in storing image data. Further suppose there is no change in images with respective to the scroll screens and no need for CPU access time.

2-2 Setting of Cycle Pattern

After the determination of the above conditions, setting of cycle patterns in the VRAM access is performed. As stated earlier, in the VRAM access, one access is performed within one pixel output time, a unit time (one cycle) being set as eight access actions corresponding to the time taken to output eight pixels in the horizontal row of a cell. As shown in Fig. 1, the VRAM access register 40 within the access circuit 31 consists of eight separate registers R1 to R8 each corresponding to one access time. In this embodiment, use is made of access commands as means for specifying to respective registers respective access actions. These access commands are each composed of a four-bit binary code and serve to specify from which scroll screen the image date are to be read. A cycle pattern is set by specifying these access commands at appropriate timing within one cycle.

The following are the contents to be set in the cycle pattern in this embodiment.

First, in order to read image data associated with the scroll screen BG0, "BG0 pattern name read" is set as a first access.

Then, readout of pattern data of the scroll screen BG0 is specified. The pattern data are comprised of cell-by-cell color codes each having a predetermined number of bits providing pixel color information among informations possessed by each pixel. With a cell configuration of eight pixels in vertical and horizontal directions, for example, the pattern data will contain color codes for 64 (8 x 8) pixels. When reading the pattern data by the VRAM access, the number of times of access actions depends on the amount of information of the pattern data. The amount of information of the pattern data in turn depends on the display conditions such as the number of bits of a color code per pixel contained in the pattern data and the size reduction ratio.

In the scroll screen BG0 using 16 colors, the color code per pixel contained in the pattern data is four bits long. Accordingly, 16-bit pattern data read by one access action contain color codes for four pixels. The predetermined amount of pattern data to be read by the VRAM access is for eight pixels (in the horizontal row of a cell). Therefore, two consecutive access actions are required in order to read the pattern data in the scroll screen BG0, which will necessitate two consecutive setting of "BG0 pattern data read".

Thereafter, with respect to the scroll screen BG1 using 256 colors, "BG1 pattern name read" is set to specify the readout of pattern name data. Then, in the readout of pattern data, the color code per pixel contained in the pattern data of the scroll screen BG1 is eight bits long. Accordingly, 16-bit pattern data contain color codes for two pixels. Therefore, four consecutive access actions are required in order to read the predetermined amount of pattern data for eight pixels, which will necessitate four consecutive setting of "BG1 pattern data read".

The cycle pattern as described above is set in a manner capable of being read in by the CPU. Setting means includes, for example, a method in which an optimum cycle pattern is determined by a unique program, or a method in which a previously prepared cycle pattern is specified into a CD-ROM, a memory cartridge or the life. The cycle pattern is read from the setting means by the CPU, and then stored from the CPU into the VRAM access register 40. Fig. 4 depicts, by way of example, a cycle pattern stored in the registers within the VRAM access register.

2-3 Operation of Present Embodiment

The operation of the access circuit for controlling the VRAM access will new be described with reference to the cycle pattern stored in the VRAM access register 40 as shown in Fig. 4.

[Procedure 1] Access Command Read

Description first will be given of the operation upon the readout of access commands from the cycle pattern. As described above, the VRAM access register of Fig. 1 consists of eight registers

R1 to R8 and receives address signals of one dot (pixel) period from the synchronous circuit 32. The address signals sequentially designate addresses in the VRAM access register of the eight registers. The VRAM access register 40 reads out in sequence access commands stored in the registers designated by the address signals. The thus read access commands are decoded in the decoder 37, and resultant read/write control signals are fed to the address selector 42 and the VRAM 12.

In compliance with the access commands read out from the VRAM access register 40, as described above, addresses in the VRAM of the image data requiring read or write are selected and fed to the VRAM. Detailed description will be given hereinbelow of the operation of generating addresses of the image data to be supplied to the VRAM.

A. Case in which Access Command is "Pattern Name Read"

When the access command read through the procedure 1 is "pattern name read" for reading out the pattern name data of the scroll screens, first generated are addresses on the VRAM 12 of the specified pattern name data (pattern name addresses). The operation of generating the pattern name addresses is as follows.

[Procedure 2] Pattern Name Address Generation

The coordinate calculation section 39 of Fig. 1 receives from the synchronous circuit 32 vertical and horizontal synchronizing signals of the scroll screens BG0 and BG1 as well as dot (pixel)-period synchronizing signals. The coordinate calculation section 39 subjects the scroll screens BG0 and BG1 to processing such as vertical and horizontal movement or rotation. Such processing is needed in the case of representing the action of an airplane by rotating or moving the background images with the position of the airplane remaining fixed, such as for example, when desiring to represent the state on the earth viewed from the airplane flying through the air.

With the assumption of scroll screens based on the pattern data and pattern name data (to be stored in the VRAM 12), the coordinate calculation section 39 performs coordinate calculations pixel by pixel in accordance with both the synchronizing signals from the synchronous circuit 32 and the instructions of the CPU 1 received through the terminal C. Thus obtained coordinate values of each pixel on the scroll screens are referred to as a pixel address.

As depicted in Fig. 5(a), the pixel address has coordinate data consisting of, for example, X-coordinate of nine bits (X0 - X8) and Y-coordinate of nine bits (Y0-Y8). Among these XY coordinate data, upper six bits (X3 - X8, Y3 - Y8) except lower three bits (X0 - X2, Y0 - Y2) are data representing a position on the scroll screen of a cell as shown in Fig. 5(d). Thus, as shown in Fig. 5(b), the X and Y coordinate data are combined with the exception of their respective lower three bits, to generate 12-bit pattern name address (X3 - X8 / Y3 - Y8) for the supply to the address selector 42.

As depicted in Fig. 5(e), on the contrary, the lower three bits (X0 - X2, Y0 - Y2) of the X and Y coordinates, among the coordinate data of the pixel address, are respectively used to represent, by the combination of codes 0 or 1 possessed by these bits, X and Y coordinate values of 64 pixels in a cell consisting of 8 x 8 pixels in vertical and horizontal directions. Among them, to the lower three bits of the X- coordinate representing eight X-coordinate values within the cell are affixed control signals representing the number of bits of a color code for each pixel as shown in Fig. 5(c). In accordance with the number of bits of the color code, they are supplied to the image data output circuit 37 for the scroll screen BG0 (four-bit color code), but to the image data output circuit 38 for the scroll screen BG1 (eight-bit color code). The Y-coordinate lower three bits (Y0 - Y2) are fed to the address selector 42 intact and used as data in generating pattern data addresses.

[Procedure 3] Address Selector - Readout Address Specification 1

Referring back to Fig. 1, the address selector 42 receives 12-bit pattern name addresses fed from the coordinates calculation section 39 as well as addresses of the VRAM 12 supplied through the terminal C. On the basis of the addresses of the VRAM 12, the address sector 42 accesses the VRAM 12 to impart the pattern name addresses to the VRAM 12.

[Procedure 4] VRAM - Pattern Name Data Readout

In the background image generation section 22 of Fig. 1, the VRAM 12 is coupled, for each of the scroll screens, to a plurality of data buffers corresponding to the kinds of the image data. Among them, the register 33 is a buffer for storing pattern name data for the scroll screen BG0, and the register 34 is a buffer for storing pattern name data for the scroll screen BG1. The VRAM 12 is supplied with pattern name addresses from the address selector 42, and reads pattern name data based on the addresses. In synchronism with this, the VRAM 12 is fed with control signals (write) from the decoder 41 whereupon the thus read pattern name data if associated with the scroll screen BG0

are stored into the register 33, and if associated with the scroll screen BG1 into the register 34.

Through the above procedures 1 to 4, the access command "pattern name read" in the VRAM access is put into execution, so that pattern name data are read and stored into the predetermined data buffer.

After the completion of the readout of the pattern name data, the access circuit 31 reads the subsequent access command in accordance with the cycle pattern stored in the VRAM access register 40. In other words, the access circuit 31 starts to read the pattern data which are cell-by-cell color data for output. The following is a description of the procedure when the access command has advanced to "pattern data read".

B. Case in which Access Command is "Pattern Data Read"

Providing that the access command read through the procedure 1 is "pattern data read", it is necessary for reading pattern data from the VRAM 12 that addresses on the VRAM 12 of the pattern data be imparted to the VRAM 12 by use of the address selector. Based on the pattern name data read from the VRAM 12 through the procedures 1 - 4, the above-described addresses are generated under the following operation.

[Procedure 5] Pattern Data Address Generation

At the time of pattern data read, in Fig. 1, the decoder 41 supplies control signals (read) to the registers 33 and 34. In response to the control signals, pattern name data are read from the register 33 (for the scroll screen BG0) or alternatively from the register 34 (for the scroll screen BG1) and sent to the address selector 42. As depicted in Fig. 6(a), the pattern name data typically contain in its lower nine bits a leading address of pattern data in the scroll screen (or the VRAM 12). The leading address serves to specify which cell to be read.

Also, from the coordinate calculation section 39, the address selector 42 receives lower three bits (Y0 - Y2) of Y-coordinate data for specifying eight Y-coordinate values within a cell, among the lower three bits of X and Y coordinate data from pixel addresses generated through the procedure 2. The lower three bits of Y-coordinate data serve to specify Y-coordinates of pixels within a cell.

A pattern data address, as shown in Fig. 6(b), is generated in the form of 12 bits obtained by combining the leading address with the lower three bits of the Y-coordinate data. As a result of this, the pattern data address functions to specify one of the eight horizontal rows within the cell. At that time, to the pattern data address are affixed a predetermined number of bits designating which read access action has read the pattern data specified by the address.

[Procedure 6] Address Selector - Readout Address Specification 2

Referring again to Fig. 1, the address selector 42 is fed with 12-bit pattern data addresses of the pattern data on the VRAM 12 generated through the procedure 5, as well as addresses of the VRAM 12 supplied from the CPU 1 through the terminal C. Based on the addresses of the VRAM 12, the address selector 42 accesses the VRAM 12 to impart the pattern data addresses to the VRAM 12.

[Procedure 7] VRAM - Pattern Data Readout

In the background image generation section 22, the VRAM 12 is coupled, for each of the scroll screens, to a plurality of data buffers for pattern data. Among them, the register 35 is a buffer for storing pattern data for the scroll screen BG0, and the register 36 is a buffer for storing pattern data for the scroll screen BG1. The VRAM 12 is supplied with pattern data addresses from the address selector 42, and reads pattern data on the basis of the addresses. In synchronism with this, the VRAM 12 is fed with control signals (write) from the decoder 41 whereupon the thus read pattern data if associated with the scroll screen BG0 are stored into the register 35, and if associated with the scroll screen BG1 into the register 36.

Through the above procedures 5 to 7, the access command "pattern data read" in the VRAM access is put into execution, so that pattern data are read and stored into the predetermined data buffer.

The above procedures 1 to 7 will ensure that image data (pattern data) read from the VRAM 12 are reconfigured in the form of pixel data, namely, pixel-by-pixel information in the image data output circuit 37 or 38. Referring to Fig. 7, detailed description will be given of the operation in outputting the pixel data.

[Procedure 8] Image Data Output

For each of the scroll screens, the image data output circuits 37 and 38 receive from the coordinate calculation section 39 both control signals for specifying the number of bits of pixel color codes and lower three bits (X0 - X2) of pixel address X-coordinate data. If control signal specifies four bits, the image data output circuit 37 is allowed to receive pattern data for two words (32 bits) read out from the register 35 for scroll screen BG0 (using 16 colors). These are pattern data for eight

pixels in the horizontal row of a cell read by two access actions in accordance with the cycle pattern. As depicted in Fig. 7(a1), the pattern data for eight pixels are segmented into eight portions (P0 - P7) every four bits from the lowest or rightmost bit. The X-coordinate lower three bits select one of eight-segmented four-bit data. In other words, one of X-coordinate values in a horizontal row is selected to specify one pixel of the eight pixels in the horizontal row. Thus, a color code for one pixel within the pattern data is specified.

As shown in Fig. 7(b1), from the register 33 are read pattern name data of the scroll screen BG0, of which upper seven bits for specifying a leading address of the color RAM 10 of Fig. 3 are added to the selected four-bit color code. Thus, pixel-by-pixel color data of 11 bits in total are formed as shown in Fig. 7 (c1).

In the case where the control signal specifies eight bits, the image data output circuit 38 is allowed to receive pattern data for four words (64 bits) read from the register 34 for the scroll screen BG1 (using 256 colors). These are pattern data for eight pixels in the horizontal row read by four access actions in accordance with the cycle pattern. As shown in Fig. 7(a2), the pattern data for eight pixels are segmented into eight portions (P0 to P7) every eight bits from the lowest or rightmost bit. The X-coordinate lower three bits selects one of the eight-segmented eight-bit data. In other words, one of X-coordinate values in a horizontal row is selected to specify one pixel of the eight pixels in the horizontal row. Thus, a color code for one pixel within the pattern data is specified.

As shown in Fig. 7(b), from the register 34 are read pattern name data of the scroll screen BG1, of which upper three bits specifying a leading address of the color RAM are added to the eight-bit color code selected by the X-coordinate lower three-bits. Thus, pixel-by-pixel color data of 11 bits in total are formed.

The pixel-by-pixel image data thus formed are output from the image data output circuits 37 or 38 via the terminal E or F into the priority circuit 24 of the display control section 23 of Fig. 3.

2-4 Effect of Present Embodiment

As described above, the access circuit of the present invention specifies access actions in the VRAM access using access commands in a predetermined form. Further, a cycle pattern is set in such a manner as to allow read into the CPU and is stored in such a manner as to allow write from the CPU, the cycle pattern setting an access command for eight access actions in one cycle of unit time. As a result, in the case of changing the cycle pattern, it is merely required to specify an access command rewriting work by the CPU. Also, in the case of providing additional VRAM access registers so as to correspond to a plurality of VRAM's, it is merely required to appropriately modify and set the access command by the CPU, thus making it possible to flexibly cope with such situation. Thus enlarged degree of freedom on setting the cycle pattern will ensure that the amount of image data is suppressed to a minimum by, for example, appropriately controlling the setting of the optimum number of colors for each of the scroll screens so as to match the display contents of each scroll screen. In this context, restricted capacity of the VRAM can be effectively utilized.

3. Other Embodiments

It will be appreciated that the present invention is not intended to be limited to the above embodiment. In view of its original aim to freely set and change the display conditions of the scroll screen, the present invention will rather allow an implementation of an access circuit having a flexible configuration in conformity with the original aim and need. Other reference examples will be described hereinbelow.

3-1 Reference Example 1 - CPU Access Setting - Addition of Access Register and VRAM

Assume for instance that in the above embodiment at least one of the scroll screens BG0 and BG1 has needed a CPU access during the display period. It is impossible in this case to secure an idle time for CPU since the above embodiment uses a single VRAM and all the contents of eight access actions per cycle are dedicated to the readout of the image data. In such case, the access circuit of the present invention is provided with additional VRAM's as needed, and with additional access registers corresponding to the VRAM's. Providing that the VRAM's are now allocated to image data for each of the scroll screens, it is possible as shown in Fig. 8 to set CPU access in one cycle even with the scroll screen BG1 using a multiplicity of colors, thus enabling new image data to be written from the CPU during the display period. Since the VRAM's and associated access registers can be additionally provided in this manner, there is no need to fixedly set useless access time which may not possibly be used to the hardware as in the prior art. In this context, burden imposed on the hardware will be alleviated.

3-2 Reference Example - Effective Application of VRAM Capacity

Further, in the above embodiment, there may be a case where the scroll screens BG0 and BG1 both make use of 256 colors or a case of increasing the number of scroll screens for display. When plenty of image data need to be read at a time in the VRAM access in this manner, it is similarly necessary to provide additional VRAM's or to subject the VRAM to bank division so as to allow the previous allocation for each of the scroll screens (Refer to 2-1 Setting of Display Conditions).

The image processing system of the present invention allows not only a simultaneous access to the plurality of VRAM's or VRAM banks but also a free setting of VRAM capacity allocation for each of the scroll screens by means of the CPU in previous consideration of, for instance, the quantity of the image data possessed by each scroll screen, or the difference in the states of use of the VRAM depending on the access frequency.

3-3 Operation and Effect

An example of usage of the VRAM of the present invention will be described hereinbelow.

[Example]

Three scroll screens BG0, BG1 and BG2 are present. At a scene A in a game, the number of colors used in the scroll screen BG2 especially increases. At another scene B in the same game, the scroll screen BG1 needs to be subjected to many display changes, the scroll screen BG2 being not displayed at all.

In such situations, two VRAM's of the present invention are provided and named VRAM-1 and VRAM-2, respectively. As illustrated in Fig. 9, at the scene A, a setting is performed for halving VRAM-1 into two banks. This depends on whether one bit within the register for controlling the RAM is 0 or 1. Then, into the VRAM-1 are stored image data for the scroll screen BG0 and scroll screen BG1 for the scene A. Also, image data of the scroll screen BG2 for the scene A are stored in the VRAM-2 not subjected to bank division. In this manner, respective VRAM's are correspondingly associated with the access registers to individually set the cycle pattern to read the image data at the scene A.

Afterwards, upon turning to the scene B, the image data for the scene B of the scroll screen BG0 are stored into the back 1a within the VRAM-1. Then the contents of the cycle pattern for the VRAM-1 are changed into ones for the read of the image data of the scroll screen BG0. Also, into the VRAM-2 are stored image data of the scroll screen BG1 for the scene B. Then, the contents of the cycle pattern of the access register for the VRAM-2 are changed into ones for the read of the image data of the scroll screen BG1. As a result of this, in the scene B, more CPU access time can be allocated to the image data of the scroll screen BG1. Simultaneously, in the scene B, the VRAM capacity can be saved with respect to the scroll screen BG2 which is not displayed at all in the scene B. In this manner, the present invention ensures an easy change of setting of the cycle pattern and hence the free and appropriate control of the allocation of the VRAM capacity in accordance with the amount of information of the image data or the necessity of access. This will contribute to an effective application of the restricted VRAM capacity.

INDUSTRIAL APPLICABILITY

According to the present invention, as described above, the cycle pattern upon the VRAM access which may vary depending on the display conditions can be more freely set and changed, thus providing an image processing system and a game machine having a higher degree of freedom allowing changeful image display.

It is also easy to decrease or increase the number of the access registers storing the cycle patterns, which will eliminate the need to previously fix the setting to the hardware to alleviate the burden on the hardware. Thus, an image processing system and a game machine can be provided capable of saving the VRAM capacity by appropriately determining the amount of information of the image data required for each of the background image, without depending on the fixed cycle pattern. Also, an image processing system and a game machine can be provided which enables the allocation of the VRAM capacity to be varied in accordance with the amount of information of the image data.

Claims

1. An image processing method in which image data for forming a foreground image are stored into a frame buffer while simultaneously storing image data for forming background images into a video RAM and in which said image data for a foreground image are read from said frame buffer in a foreground image processing section in synchronism with the readout of said image data for background images from said video RAM in a background image processing section, whereby at the same timing said foreground image and background images are generated and superimposed with each other

to be output in the form of a synthetic image, said method comprising the steps of:

specifying the contents of concrete actions to be imparted to said video RAM in order to perform readout and write-in of said background image data;

setting said specified contents of actions at given unit time intervals, said setting being instructed by a CPU; and

accessing said video RAM in conformity with an instruction from said CPU.

2. An image processing method in which one ore more video RAM's are provided for storing image data for background images and in which said video RAM's store image data and are simultaneously accessed, said method comprising the steps of:

by means of a CPU, specifying the readout of said video RAM's and image data stored in said video RAM's.

3. An image processing method according to claim 2, wherein

said video RAM is segmented into two banks which are plurality of RAM portions each having the same capacity, and wherein

said CPU specifies the readout of said banks and image data stored in said banks.

4. An image processing system including a foreground image processing means which stores image data for forming a foreground image into a RAM and develops said image data into a frame buffer and at a predetermined timing reads out said image data for a foreground image from said frame buffer, a background image processing means which reads out image data for forming background images from a video RAM, a priority determining means which determines display priority among image data for a foreground image transferred from said foreground image processing means and image data for background images transferred from said background image processing means, and an output means which outputs said image data for a foreground image and background images in conformity with said priority,

said system comprising:

a specifying means for specifying actions reading or writing image data stored in said video RAM;

a first setting means for setting at given unit time intervals said actions specified by said specifying means;

a storage means for storing the contents of said actions set at given unit time intervals by said first setting means;

an access control means for controlling access to said video RAM in compliance with the contents stored in said storage means; and

a bit-number output control means for performing output control by the number of bits of predetermined data within image data in accordance with the amount of information differing for each of background images.

5. An image processing system according to claim 4, wherein said access control means includes:

a conversion means for converting a specification by said specifying means into a control signal; and

an address selection means for selecting an address on said video RAM of image data read out from said video RAM.

6. An image processing system according to claim 5, wherein

said address selection means includes:

a first generation means for generating an address on said video RAM of pattern name data; and

a second generation means for generating an address on said video RAM of pattern data.

7. An image processing system according to claim 4, wherein

in a video RAM access for reading image data for background images by accessing said video RAM storing as said image data both pattern data composed of predetermined number of pixel informations and pattern name data for designating positions in the background images of said pattern data defining images to be displayed,

an access command is used as a specification means for specifying the action reading or writing said pattern data or pattern name data.

8. An image processing system according to claim 7, wherein

said access command is a binary code consisting of a predetermined number of bits.

9. An image processing system according to claim 7, wherein

in said video RAM access,

as a setting means for setting in one cycle unit during the display period said action specified by said access command, a cycle pattern is set in the form allowing read-in by said CPU.

10. An image processing system according to claim 7, wherein

in said video RAM access,

a video RAM access register is used as a storage means for storing said cycle pattern.

11. An image processing system according to claim 7, wherein

in said video RAM access,

access to said video RAM is controlled in conformity with said access command sequentially read from said cycle patterned in said access register.

12. An image processing system according to claim 4, wherein

in the case of using a plurality of video RAM's or a plurality of banks for storing image data for background images,

said system further comprising:

a second setting means for setting whether said video RAM is to be divided into a plurality of banks or not; and

an access means allowing simultaneous access to said plurality of video RAM's or to said plurality of banks, by allocating a plurality of said storage means to each of said plurality of video RAM's or each of said plurality of banks of said video RAM.

13. A game machine including a foreground image processing means which stores image data for forming a foreground image into a RAM and develops said image data into a frame buffer and at a predetermined timing reads out said image data for a foreground image from said fame buffer, a background image processing means which reads out image data for forming background images from a video RAM, a priority determining means which determines display priority among image data for a foreground image transferred from said foreground image processing means and image data for background images transferred from said background image processing means, and an output means which outputs said image data for a foreground image and background images in conformity with said priority,

said game machine comprising:

a specifying means for specifying actions reading or writing image data stored in said video RAM;

a first setting means for setting at given unit time intervals said actions specified by said specifying means;

a storage means for storing the contents of said actions set at given unit time intervals by said first setting means;

an access control means for controlling access to said video RAM in compliance with the contents stored in said storage means; and

a bit-number output control means for performing output control by the number of bits of predetermined data within image data in accordance with the amount of information differing for each of background images.

14. A game machine according to claim 13, wherein

said access control means includes:

a conversion means for converting a specification by said specifying means into a control signal; and

an address selection means for selecting an address on said video RAM of image data read out from said video RAM.

15. A game machine according to claim 14, wherein

said address selection means includes:

a first generation means for generating an address on said video RAM of pattern name data; and

a second generation means for generating an address on video RAM of pattern data.

16. A game machine according to claim 13, wherein

in a video RAM access for reading image data for background images by accessing said video RAM storing as said image data both pattern data composed of predetermined number of pixel informations and pattern name data for designating positions in the background images of said pattern data defining images to be displayed,

an access command is used as a specification means for specifying the action reading or writing said pattern data or pattern name data.

17. A game machine according to claim 16, wherein

said access command is a binary code consisting of a predetermined number of bits.

18. A game machine according to claim 16, wherein

in said video RAM access,

as a setting means for setting in one cycle unit during the display period said action specified by said access command, a cycle pattern is set in the form allowing read-in by said CPU.

19. A game machine according to claim 16, wherein
in said video RAM access,
a video RAM access register is used as a storage means for storing said cycle pattern.

20. A game machine according to claim 16, wherein
in said video RAM access,
access to sad video RAM is controlled in conformity with said access command sequentially read from said cycle pattern stored in said access register.

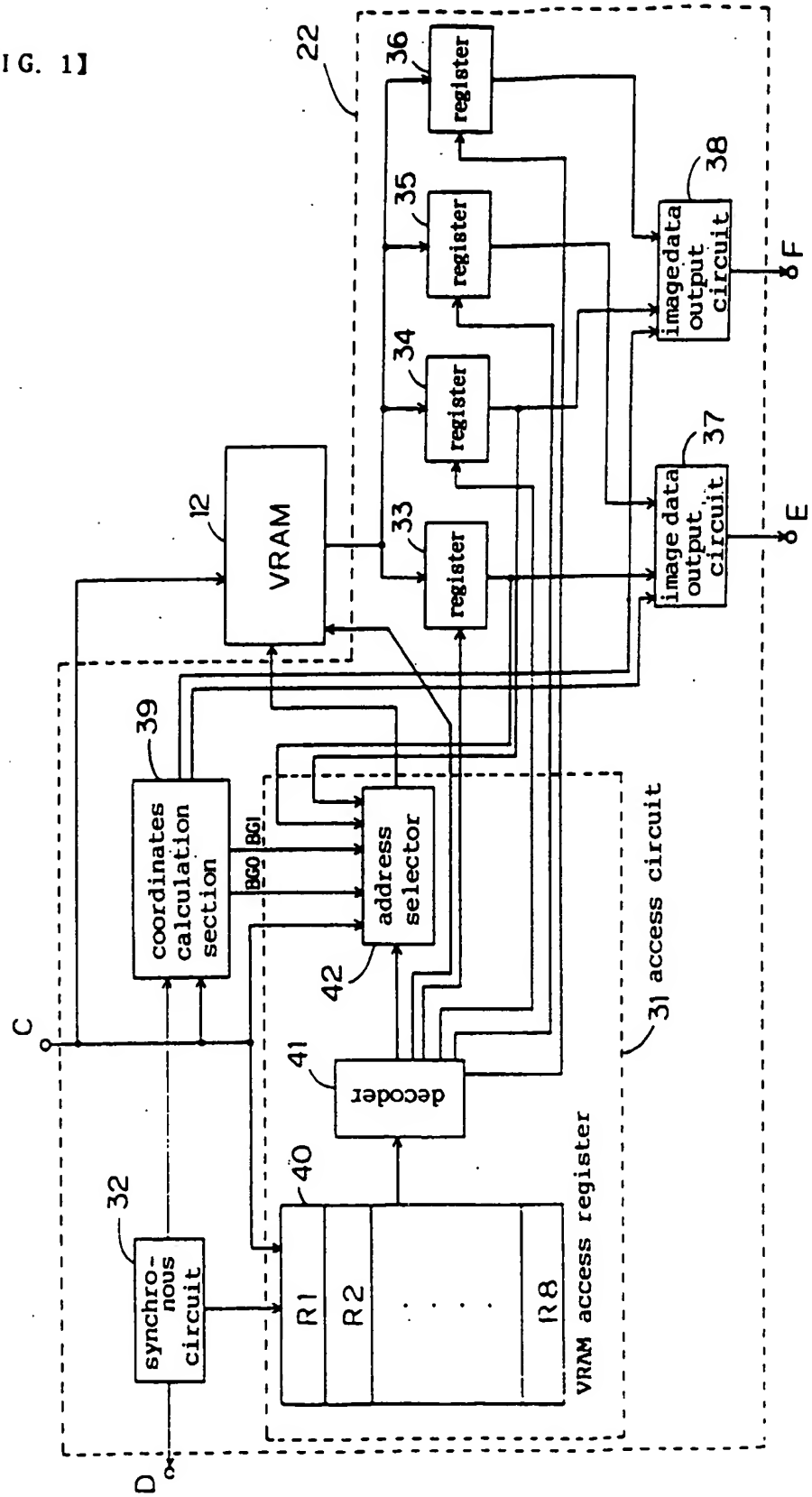
21. A game machine according to claim 13, wherein
in the case of using a plurality of video RAM's or a plurality of banks for storing image data for background images,
said game machine further comprising:
a second setting means for setting whether said video RAM is to be divided into a plurality of banks or not; and
an access means allowing simultaneous access to said plurality of video RAM's or to said plurality of banks, by allocating a pluralaity of said storage means to each of said plurality of video RAM's or each of said plurality of banks of said video RAM.

Amended claims

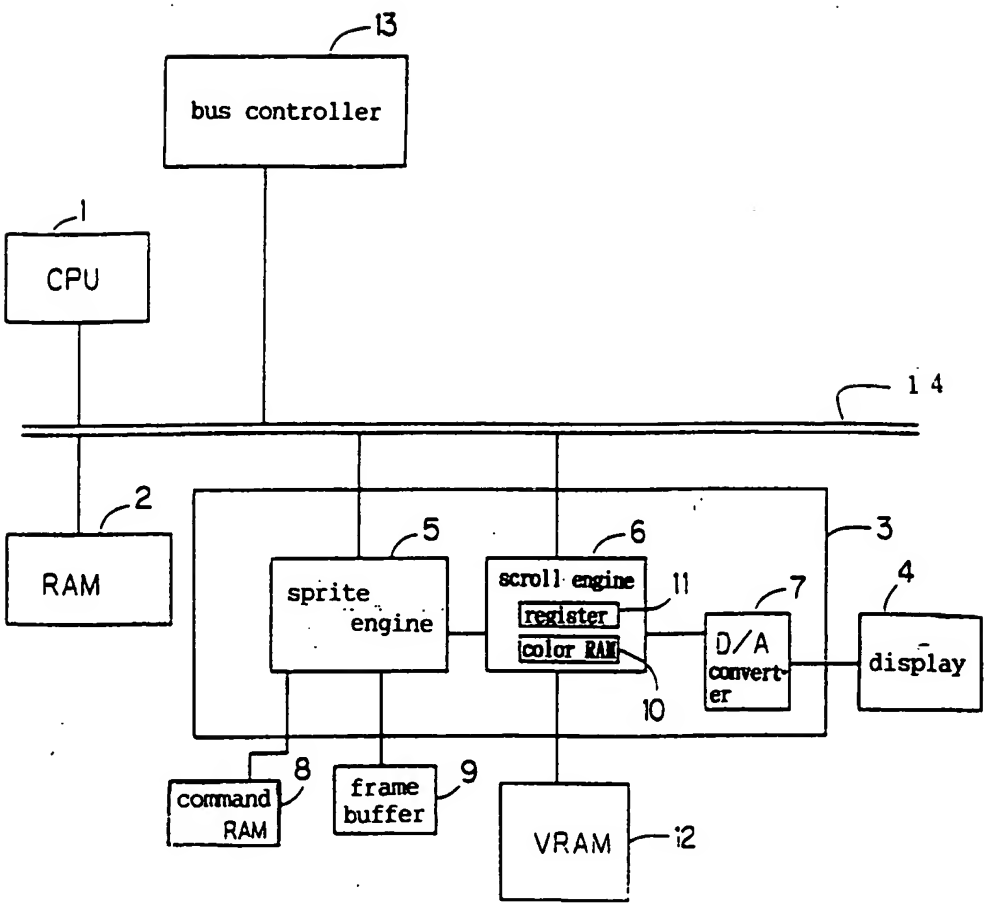
2. An image processing method according to claim 1, wherein
at least one said video RAM is provided,
said method further comprising the steps of:
specifying concrete contents of actions provided to perform readout and write-in of image data for background images, to each said video RAM on the basis of the access frequency required for each said video RAM;
individually setting said specified contents of action at given unit time intervals, the setting being instructed by a CPU; and
accessing each said video RAM in conformity with instructions from said CPU.

3. An image processing method according to claim 2, wherein
said video RAM is divided into two banks which are plurality of RAM portions having the same capacity,
said method further comprising the steps of:
specifying concrete contents of actions provided to perform readout and write-in of image data for background images, to each of said banks on the basis of the access frequency required for each of said banks;
individually setting said specified contents of action at given unit time intervals, the setting being instructed by a CPU; and
accessing each of said banks in conformity with instructions from said CPU.

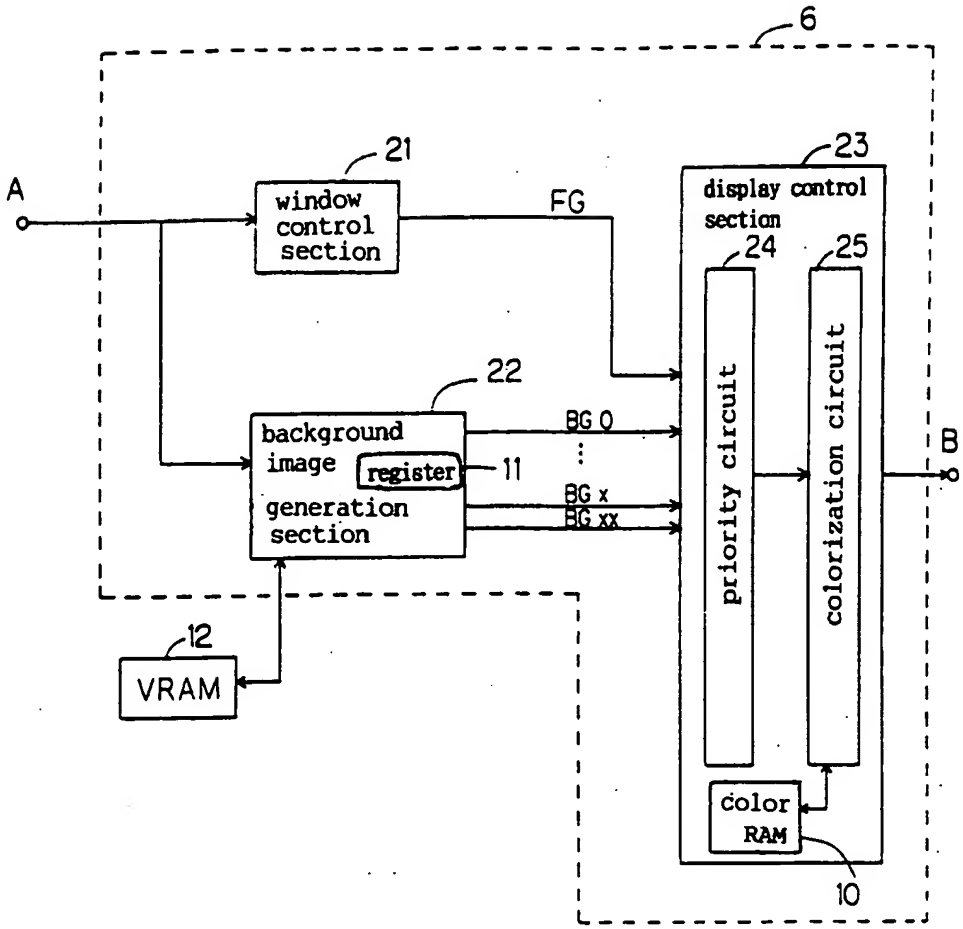
【FIG. 1】


22
36
register
35
register
34
register
33
register
38
imagedata output circuit
F
37
image data output circuit
E
12
VRAM
39
coordinates calculation section
BG1
BG0
address selector
42
C
41
decoder
31 access circuit
40
32
synchro-nous circuit
R1
R2
R8
VRAM access register
D

【FIG. 2】


13
bus controller
1
CPU
14
2
RAM
5
sprite engine
6
scroll engine
11
register
color RAM
10
7
D/A converter
3
4
display
8
command RAM
9
frame buffer
VRAM
12

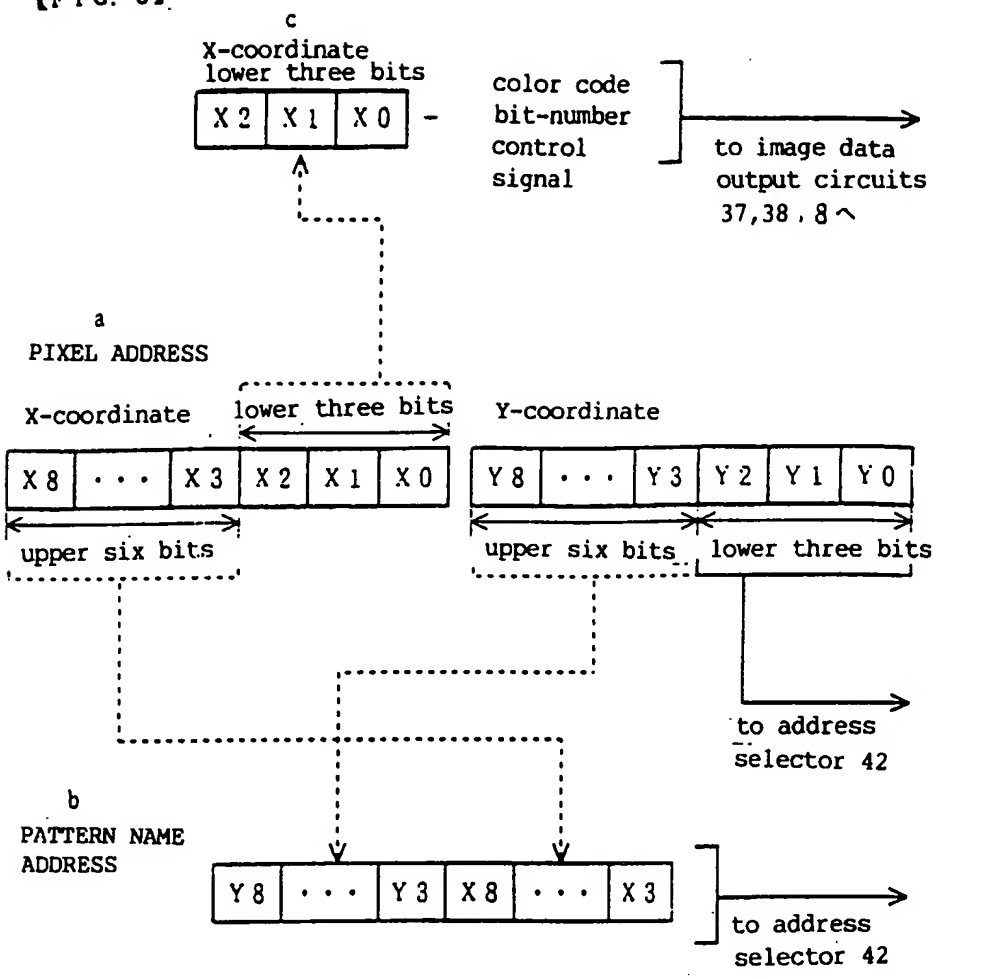
【FIG. 3】

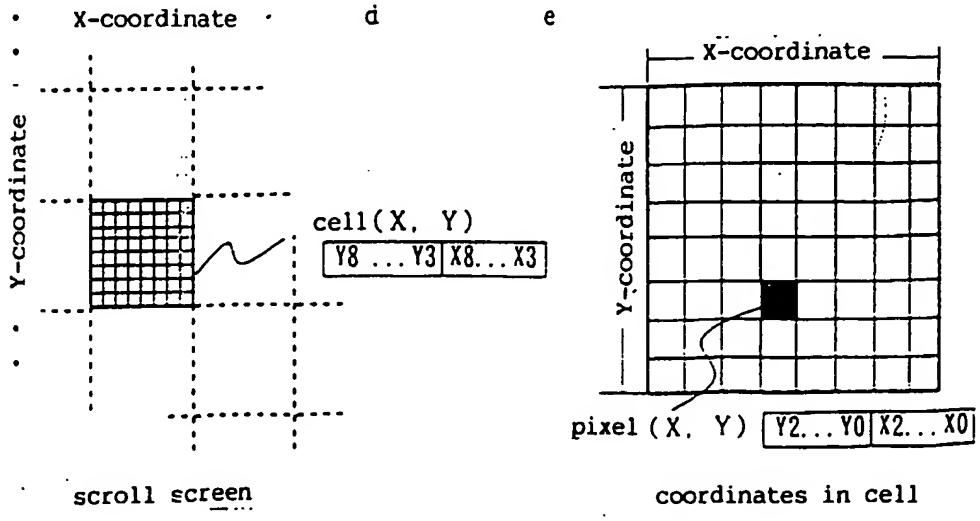

6
21
23
A
window control section
FG
display control section
24
25
priority circuit
colorization circuit
22
background image register 11 generation section
BG 0
BG x
BG xx
B
12
VRAM
color RAM
10

【FIG. 4】

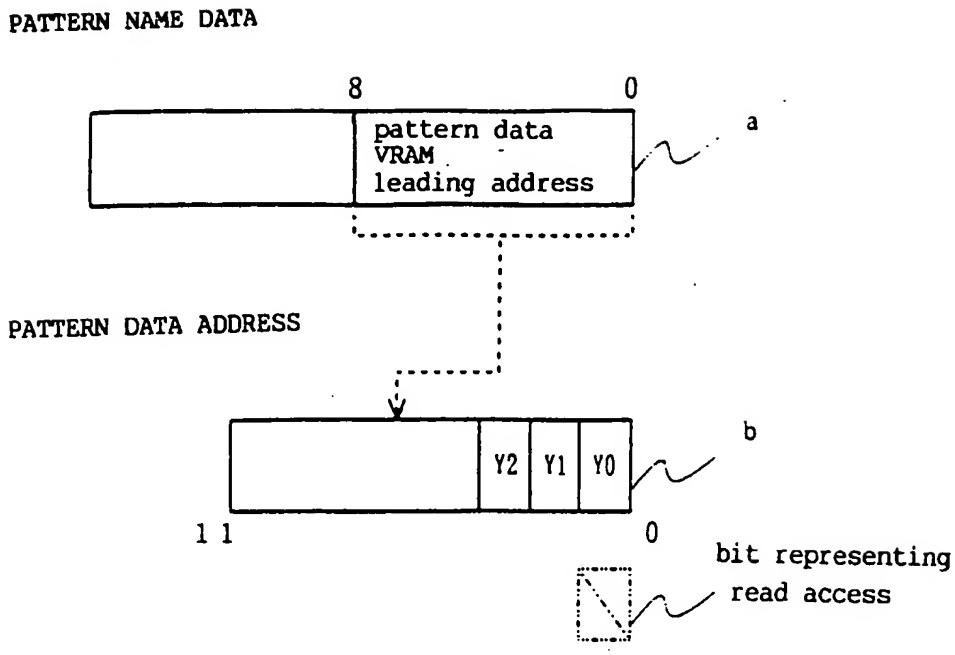
Access No.	Register No.	Access Contents
A1	R1	BG0 pattern name read
A2	R2	BG0 pattern data read 1
A3	R3	BG0 pattern data read 2
A4	R4	BG1 pattern name read
A5	R5	BG1 pattern data read 1
A6	R6	BG1 pattern data read 2
A7	R7	BG1 pattern data read 3
A8	R8	BG1 pattern data read 4

【FIG. 5】

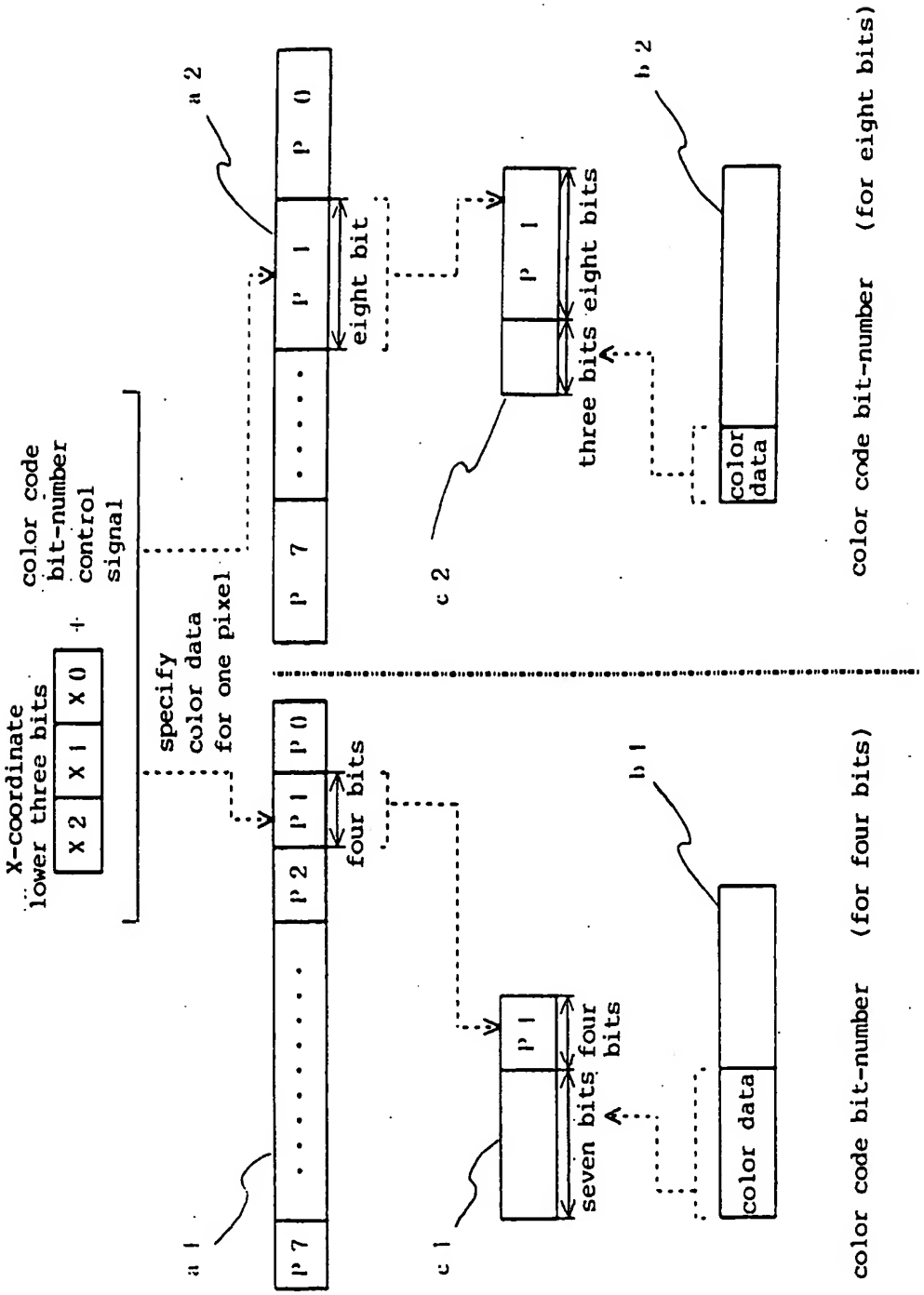

c
X-coordinate lower three bits
X2 X1 X0
color code bit-number control signal
to image data output circuits 37,38,8
a
PIXEL ADDRESS
X-coordinate
lower three bits
Y-coordinate
X8 ... X3 X2 X1 X0
Y8 ... Y3 Y2 Y1 Y0
upper six bits
upper six bits
lower three bits
to address selector 42
b
PATTERN NAME ADDRESS
Y8 ... Y3 X8 ... X3
to address selector 42


X-coordinate
d
e
Y-coordinate
cell(X, Y)
Y8 ... Y3 X8 ... X3
X-coordinate
Y-coordinate
pixel (X, Y)
Y2 ... Y0 X2 ... X0
scroll screen
coordinates in cell

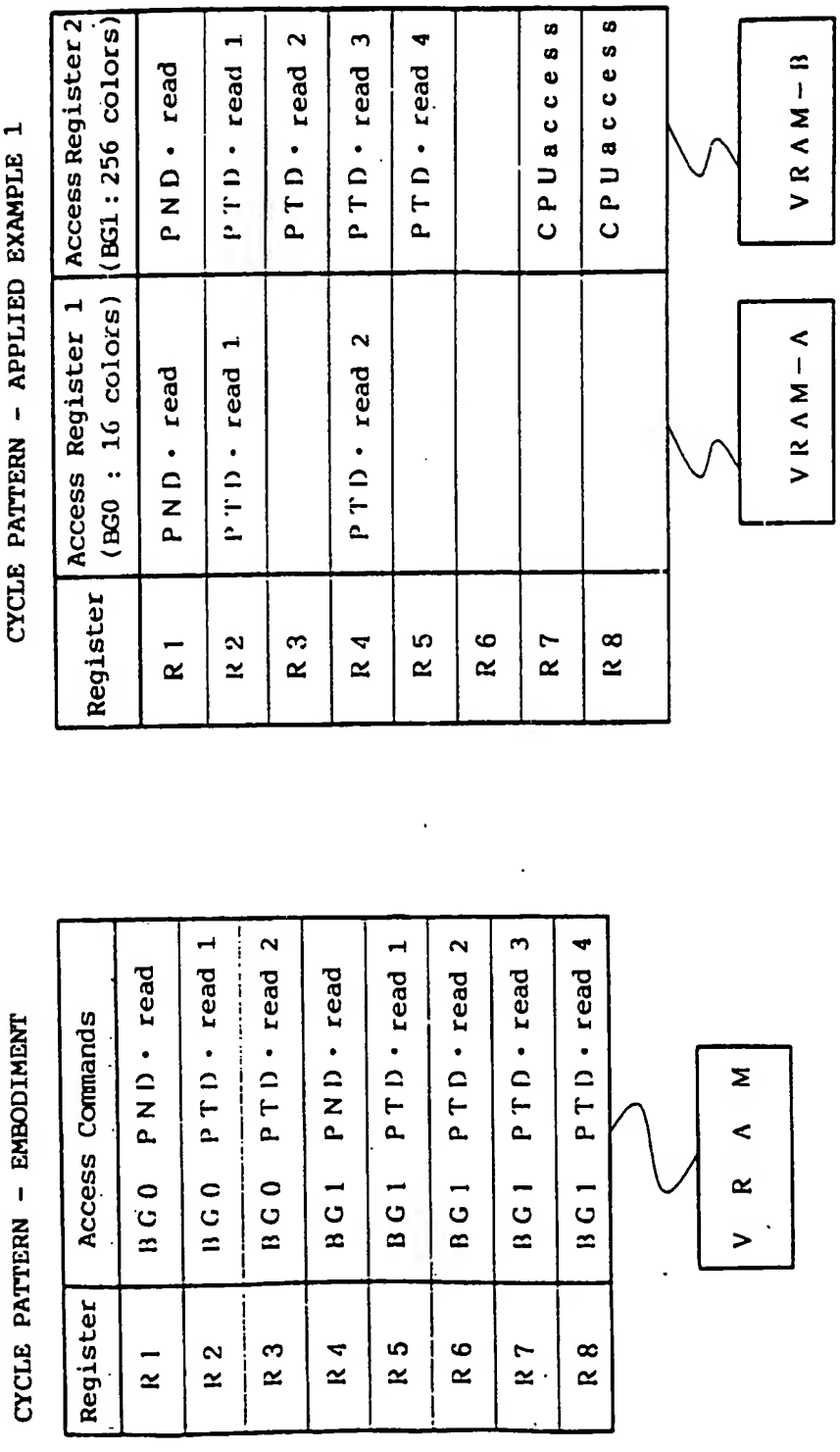
【F I G. 6】


PATTERN NAME DATA
8
0
pattern data
VRAM
leading address
a
PATTERN DATA ADDRESS
Y2
Y1
Y0
b
1 1
0
bit representing
read access

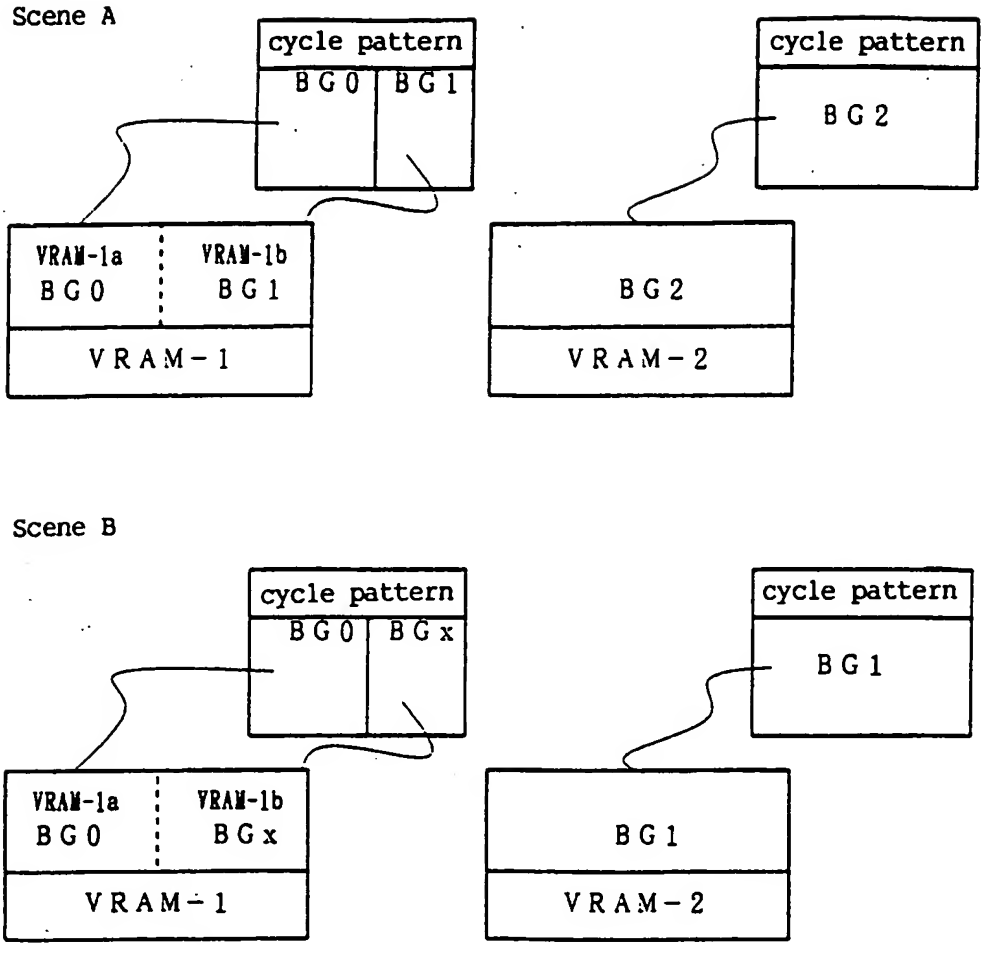
【FIG. 7】


X-coordinate lower three bits
X 2
X 1
X 0
color code bit-number control signal
specify color data for one pixel
a 2
P 7
P 0
eight bit
four bits
a 1
P 2
P 1
P 0
c 2
three bits
eight bits
c 1
seven bits
four bits
b 2
b 1
color data
color code bit-number (for eight bits)
color code bit-number (for four bits)

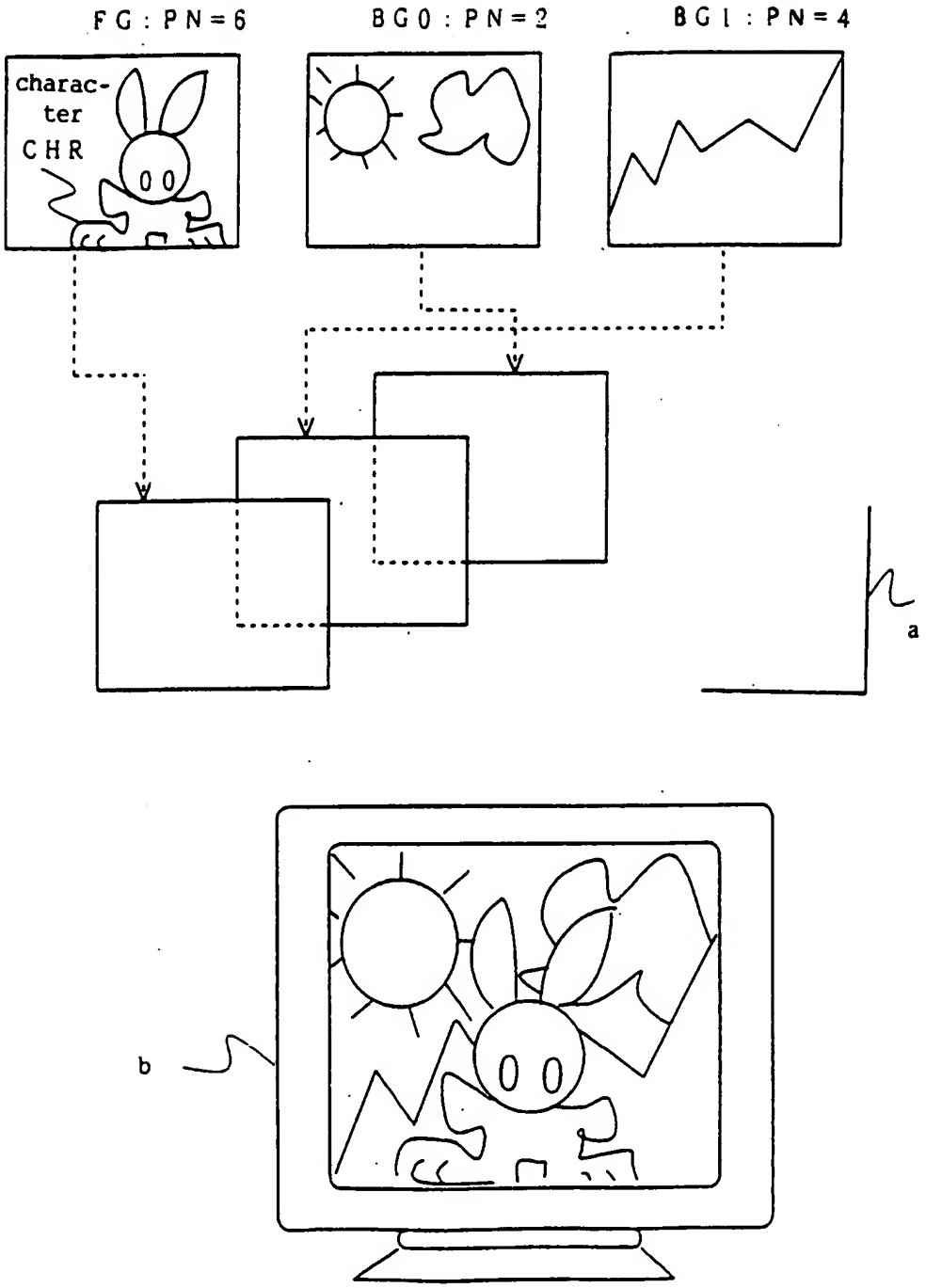
【FIG. 8】


CYCLE PATTERN - EMBODIMENT
Register
Access Commands
R1
BG0 PND • read
R2
BG0 PTD • read 1
R3
BG0 PTD • read 2
R4
BG1 PND • read
R5
BG1 PTD • read 1
R6
BG1 PTD • read 2
R7
BG1 PTD • read 3
R8
BG1 PTD • read 4
VRAM
CYCLE PATTERN - APPLIED EXAMPLE 1
Register
Access Register 1 (BG0 : 16 colors)
Access Register 2 (BG1 : 256 colors)
R1
PND • read
PND • read
R2
PTD • read 1
PTD • read 1
R3
PTD • read 2
R4
PTD • read 2
PTD • read 3
R5
PTD • read 4
R6
R7
CPUaccess
R8
CPUaccess
VRAM-A
VRAM-B

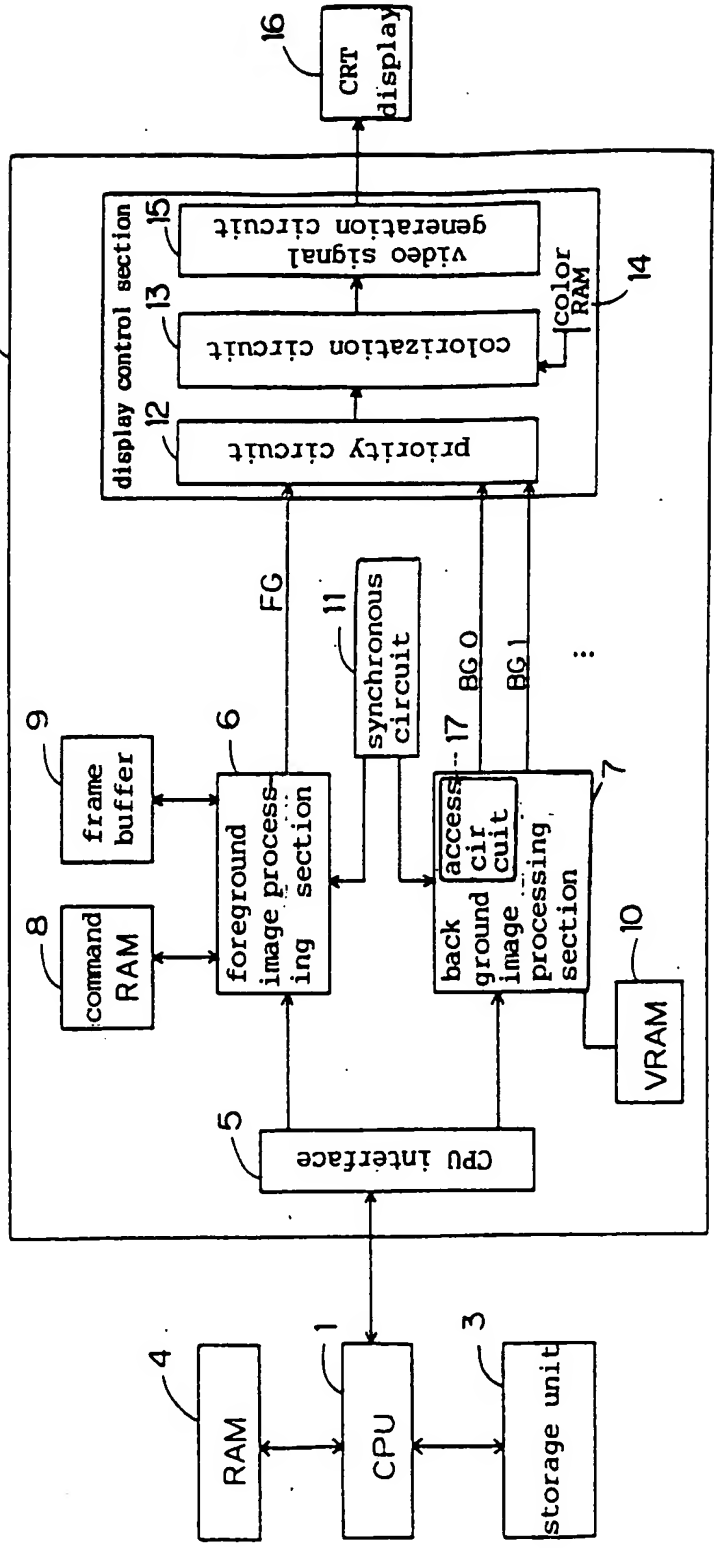
【FIG. 9】


Scene A
cycle pattern
BG0
BG1
cycle pattern
BG2
VRAM-1a
BG0
VRAM-1b
BG1
VRAM-1
BG2
VRAM-2
Scene B
cycle pattern
BG0
BGx
cycle pattern
BG1
VRAM-1a
BG0
VRAM-1b
BGx
VRAM-1
BG1
VRAM-2

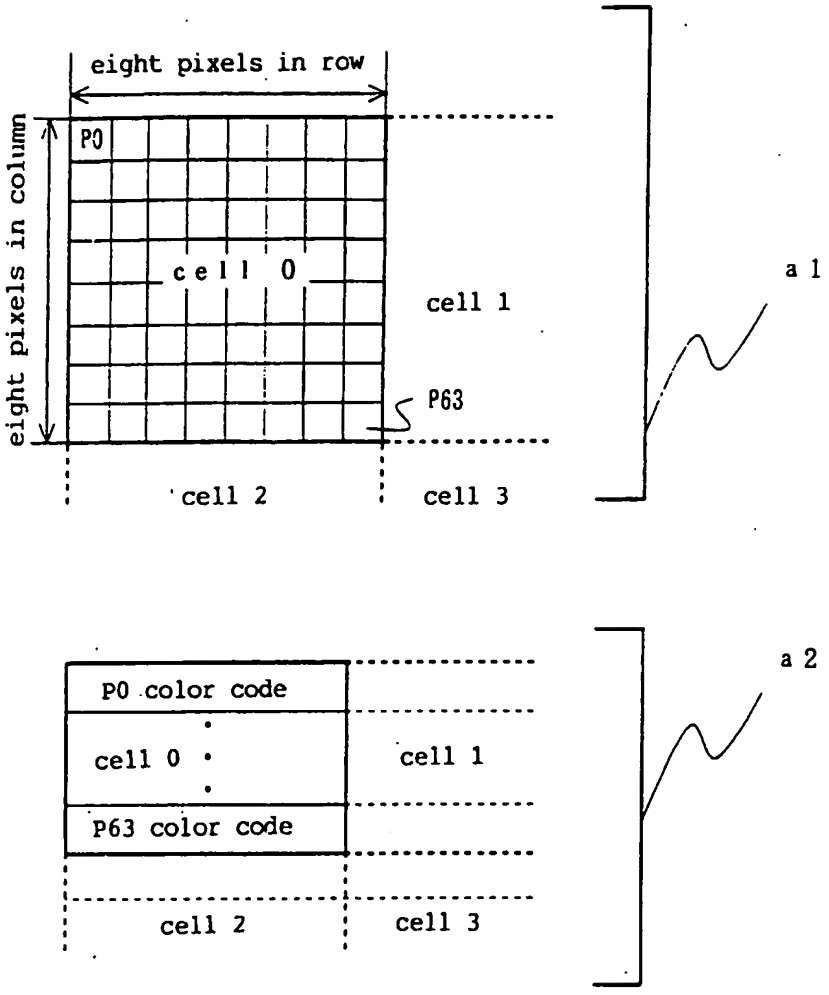
【FIG. 10】



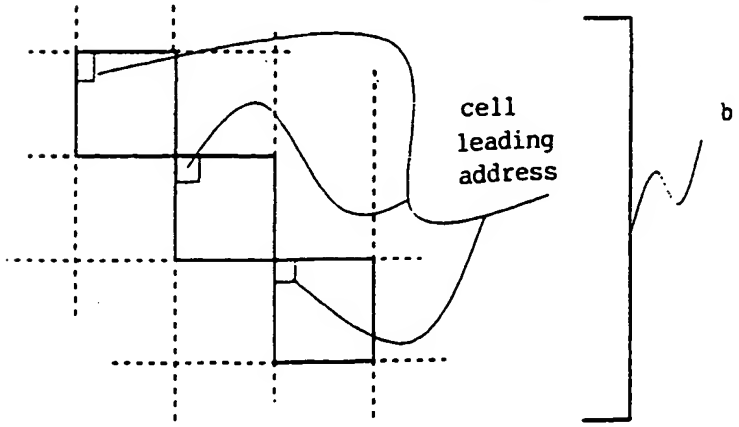
【FIG. 11】


16
CRT display
2
display control section
15
video signal generation circuit
13
colorization circuit
color RAM
14
12
priority circuit
FG
11
synchronous circuit
BG 0
BG 1
9
frame buffer
6
foreground image processing section
17
access circuit
7
back ground image processing section
8
command RAM
10
VRAM
5
CPU interface
4
RAM
1
CPU
3
storage unit

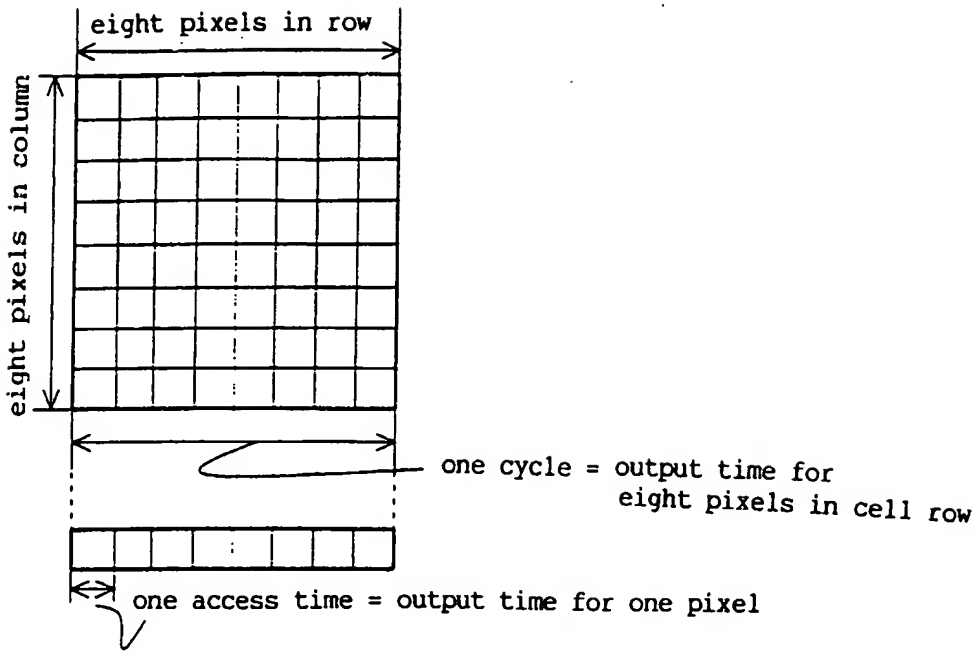
【FIG. 12】



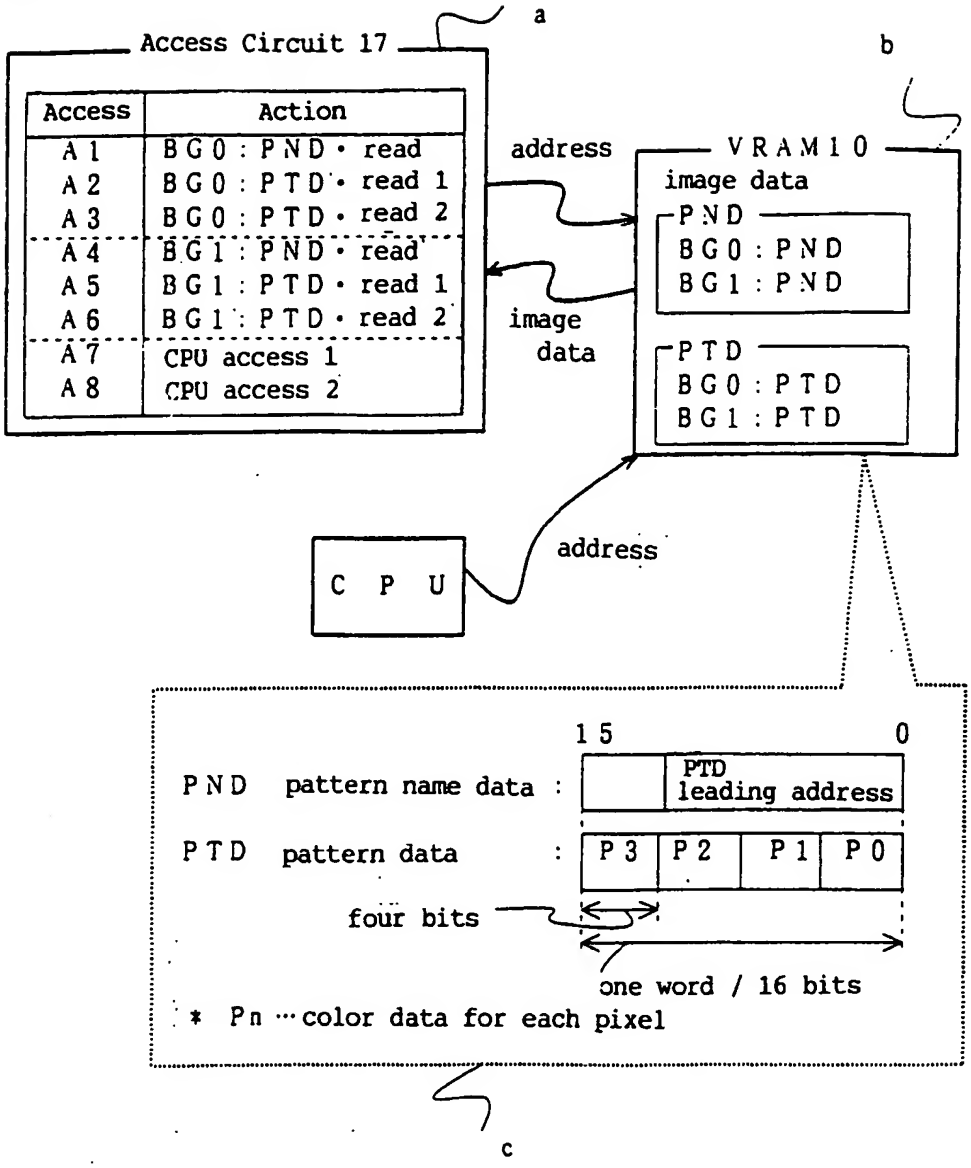
Picture Configuration of Background Image



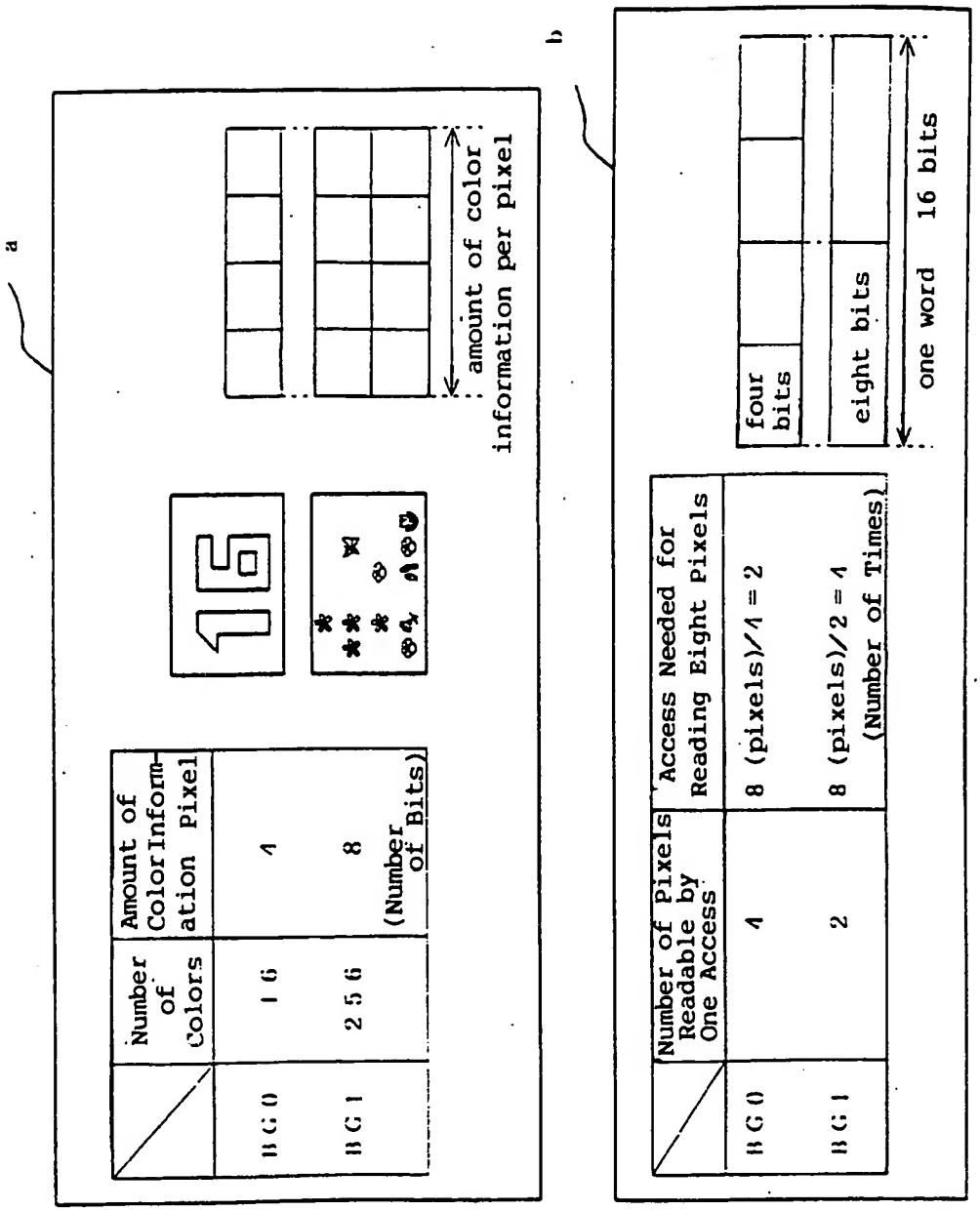
[FIG. 13]


eight pixels in row
eight pixels in column
one cycle = output time for
eight pixels in cell row
one access time = output time for one pixel

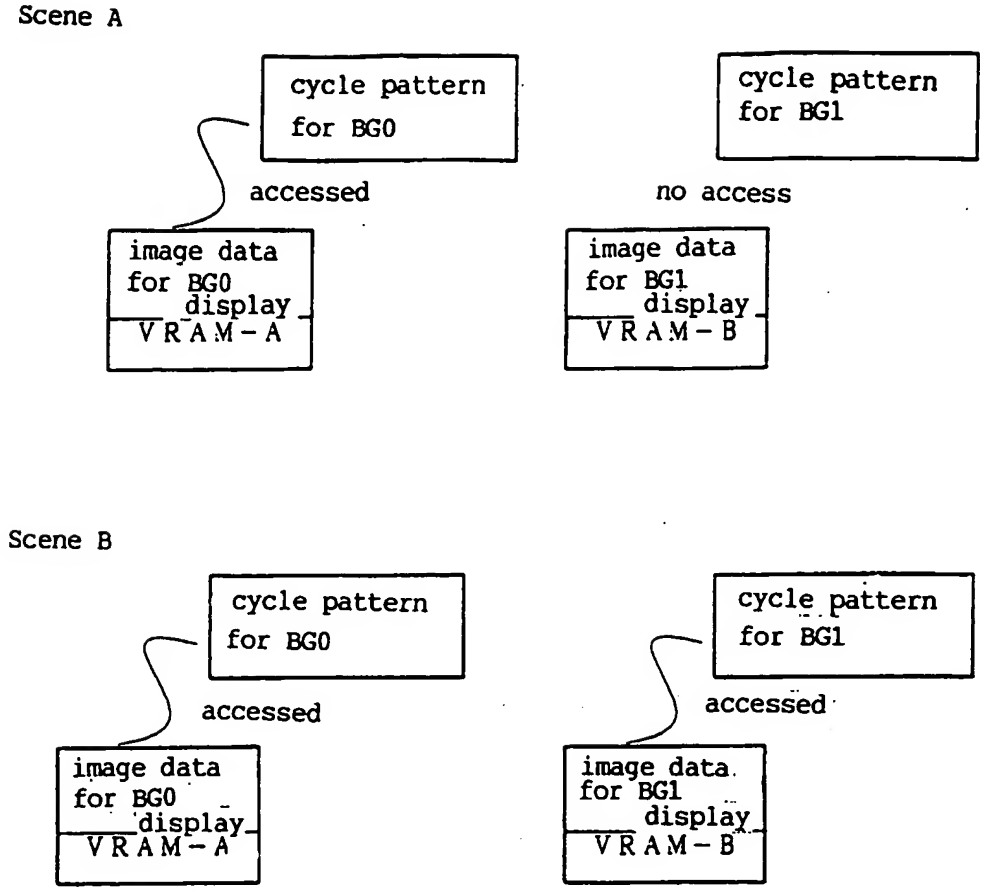
【FIG. 14】


a
Access Circuit 17
Access
Action
A1
BG0 : PND • read
A2
BG0 : PTD • read 1
A3
BG0 : PTD • read 2
A4
BG1 : PND • read
A5
BG1 : PTD • read 1
A6
BG1 : PTD • read 2
A7
CPU access 1
A8
CPU access 2
address
image data
b
VRAM10
image data
PND
BG0 : PND
BG1 : PND
PTD
BG0 : PTD
BG1 : PTD
address
CPU
15
0
PND pattern name data :
PTD leading address
PTD pattern data :
P3
P2
P1
P0
four bits
one word / 16 bits
* Pn ··· color data for each pixel
c

【FIG. 15】


a
Number of Colors
Amount of Color Information Pixel
BG0
16
4
BG1
256
8
(Number of Bits)
amount of color information per pixel
b
Number of Pixels Readable by One Access
Access Needed for Reading Eight Pixels
BG0
4
8 (pixels)/4 = 2
BG1
2
8 (pixels)/2 = 4
(Number of Times)
four bits
eight bits
one word 16 bits

[FIG. 16]


Scene A
cycle pattern for BG0
accessed
image data for BG0 display
VRAM-A
cycle pattern for BG1
no access
image data for BG1 display
VRAM-B
Scene B
cycle pattern for BG0
accessed
image data for BG0 display
VRAM-A
cycle pattern for BG1
accessed
image data for BG1 display
VRAM-B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP94/01066

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl^5 G09G5/36, G06F15/66, 450

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. Cl^5 G09G5/00-5/36, G06F15/66, 450, A63F9/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1926 - 1994
Kokai Jitsuyo Shinan Koho 1971 - 1994

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, A, 2-503238 (Comodoll Amiga Inc.), October 4, 1990 (04. 10. 90) & WO, A1, 88/490	1-2

☐ Further documents are lised in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search	Date of mailing of the international search report
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